PAMELA KUMAR

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Nationality/Visa : US Citizen / OCI (Overseas Citizen of India)

Master of Science (1985): Rutgers University, Piscataway, NJ. USA
Electrical Engg. (Computer Arch., Comp Sc & Communications)

EGMP- IIM Bangalore 2006 (3rd Rank)
Founder, Vice President – Cloud Computing Innovation Council of India
IEEE Roles - Standards Association Board of Governors, Regon10 Industry Relations, Charles Steinmetz Awards Committee, ANTS Conference - General Co-Chair(2016), Panel Chair (2014/15), Bangalore Section – Vice Chair, Chair Computer Society, Executive Committee Member – India Semiconductor Association
Founding Member – RFID Consortium; Medical Electronics Forum, FICCI

Bachelor of Engineering Electronics & Electrical Communication(1983): Punjab Engineering College, Chandigarh , INDIA

Merit Scholarship, Best Project Award – Punjab Engg College
STG Rep – IBM Technical Leadership Team, IBM Distinguished Engineer Review Board (4yrs), IBM External Honours review board
4 Patents awarded by USPTO
Current Board Appointments – Indian Financial Technology & Allied Services (IFTAS); PEC University
Visiting Professor, Bharti Chair for Telecom & IT Research – UIET, Panjab University

EMPLOYMENT

Present – VP and Founding Chairperson**, Cloud Computing Innovation Council of India**
2014 to 2015 HP : Senior Director, Advanced Systems Engg. Lab, HP Enterprise R&D India
2007 to 2013: IBM : India Systems and Technology Lab.
July 2012 to Feb 2013 - Leader, Technical Vitality
2010 to 2012 - Director, Storage & Networking Lab
2007 to 2010 - Director, Semiconductor & Technology Lab
1999 to 2007 : Texas Instruments , India
Sept. 2005 onwards: Director, Strategic Programs
2003 to 2005: Director, Cellular Systems SW R&D
2001 to 2003: General Manager, Broadband Communications
1999 to 2001: Program Manager, Cable Broadband Communications
1998 to 1999: Design Manager, Networking Products, Alliance Semiconductor, India.
1996 to 1998: Executive Director, Network Programs India (NPI),
1989 to 1996: C-DOT (Centre for Development of Telematics)
1996: Visiting Consultant (on leave from C-DOT), Network Programs, Piscataway NJ, USA.
1993 to 1996: Program Manager, Parallel Processing Group, C-DOT, Bangalore
Additional charge: Program Manager, CAD Group (for 6 months), C-DOT, Bangalore
1989 to 1992: Research Engineer, Switching Division, C-DOT, Bangalore,.
1985 to 1988: **Member of Technical Staff, AT&T Information Systems, Holmdel, NJ, USA.**

RELEVANT SKILLS

1. Strategic Roles:
   - Mentoring Start-ups, Founding organisations, Member on Boards of Companies, Academic Institutions and Professional bodies
   - Ecosystem Analysis for R&D and M&A strategy – collaboration platform, negotiating charter, work partitioning, working model
   - Mapping market ecosystem & defining business development and customer support strategy for India markets
   - Determination of product line strategy for a business unit and pioneering new technology into the organisation
2. Product Life Cycle Management: Managed all aspects of product development :
   - Product-line road map and product concept: working with marketing, standards bodies, technology and research groups
   - Prototyping and development : hardware (including mechanical) & software development, system engineering, system test
   - Product deployment & support : field trials, certification, installation, technology transfer, production support and customer support
3. Organisation Building: Established from scratch, and managed, up to 750+ member organizations for complete product development as well as competency based design centres delivering to different product lines. Directly managed :
   - Organizational framework spanning across industry & competency specialization, technical vitality, innovation, sales & marketing support, talent acquisition, leadership development, execution & operational excellence
   - R&D functions: technology office, data-center & telecom infrastructure, computer & communication systems, embedded systems, microprocessor architecture, semiconductor process development, application software, system software, board design, power supply design, mechanical design, IC and ASIC design; system integration and testing.
   - Business and Support functions: business development, customer support, sales and marketing, program management, process and quality, CAD support and tools, IT support, technical vitality, finance & purchase, HR & admin .
   - Working models with vendors, 3rd parties, various functional groups in matrix organizations and off-site locations in multi-national operations
4. Domain Expertise:
   - Telecom, Networking, Broadband, Wireless, RFID, IoT Solutions, Data Center Infrastructure technologies
   - Hi-Performance Computing, Storage, Networking, Processor & Memory Technologies,: concepts, evolution, architecture and design
5. Customer Account Management
6. Hands-on experience in Software Development:
   - Generation of user requirements, functional specifications, architectural design - using client-server and object oriented models, test specifications, Integration testing and release management
   - Establishment of SW Engg and Project Management processes
   - Experience in C- programming, technical documentation
7. Hands-on experience in hardware development:
   - System specification generation, architectural analysis, behavioural and performance modelling
   - System, sub-system architecture, hardware-software partitioning. Logic design, component selection, test vector generation, timing, power and thermal analysis, functional and fault simulation
   - Front-end and Back-end full-custom IC design; Front-end ASIC design.
   - Multi-layer high-speed PCB design, vendor selection, prototyping, testing & system integration of boards, ASICs

DETAILS OF WORK EXPERIENCE:

***Oct 2012 to present* – Chair, Vice President CLOUD COMPUTING INNOVATION COUNCIL of India (CCICI)**

CCICI is a Collaborative Platform bringing together technical experts from across Industry, Academia, Government Labs and professional bodies to promote Innovation around Cloud computing in India. This has evolved into a one of a kind initiative in India, in the last year the key accomplishments have been:

1. Providing Consultation to DeitY on – Cloud Strategy, Cloud Management Office, RfP for Cloud Service Providers, Rules & RfP for Digital Locker, Multi-vendor framework for Cloud Services
2. Formation of the IoT for Smart Cities Task Force to provide- UseCase Analysis, Reference Architecture and RfP Guidelines to DeitY to enable City Commissioners to accelerate deployment for the MoUD driven SMART City Challenge
3. "Cloud Computing Adoption and Innovation in India – An Approach to a Road-map Whitepaper v1.0&2.0" released – ~ 200 page document with contributions from 80+ members, outlining the purpose and scope.
4. Scope, Working Model and Governance established - 270+ members (90+ affiliations), 16 Technical Working Groups, 6 Task Forces, Executive Committee, Advisory Board, Governing Board.11 workshops conducted. Website launched – www.ccici.in
5. Affiliations – IEEE–SA Industry Connections Program, IEEE-CS. Active engagement with National Innovation Council and Department of Electronics & Information Technology, NIST, SNIA, CeG Karnataka etc.

June 2013 to May 2015 – Hewlett Packard Enterprise Group, India - Bangalore

Senior Director, Advanced Systems Engineering Lab, Converged DataCenter Infrastructure (CDI) R&D:

1. Established the Center of Excellence for Deployment – Responsible for the entire suite of HP's Deployment & Provisioning Products. Also driving the road map and Innovation for the next generation CDI products (30+ patent submissions)
2. Developed and delivered the Data Center Simulator for the Next Generation CDI platform. Set up the team for manageability module for the CDI direct attach Storage subsystem.
3. Actively contributed to the Employee Engagement Initiative and mentored the University Relations Initiative.

June 2007 to Feb 2013: IBM, India – Bangalore

Aug 2010 to July 2012: **Director, India Storage & Networking Lab**, IBM Systems and Technology group. I helped establish the foundational structure for these labs which are focused on driving some key emerging technologies in the FCoE (Fibre Channel over Ethernet) and SONAS (Scale Out NAS) areas.

A leadership, operational and governance model is in place with the objective of establishing a world class product leadership lab in these emerging areas. Significant product architecture and global leadership roles are being driven by the India Lab. Noticeable business impact in less than 1.5 years :

1. Primary role in the delivery of the organically developed complex SONAS – Storage product.
2. Collaboration with research to implement the innovative clustered file systems over a WAN in the form of the Active Cloud Engine, enabling a 2 year+ leapfrog over competition.
3. Driving the roadmap on Cloud enablement(Security, Authentication, Multi-tenancy, REST, Object-Store) of Scale Out NAS product.
4. The networking lab drove the development of the FCoE interface and the Software Defined Networking line of products

June 2007- Aug 2010: **Director, India Systems and Technology LAB** my primary contribution has been to grow and establish the Semiconductors & Technology LAB in India (500+ people) spanning across :

1) Semiconductor R & D : this department is engaged in :
    a. developing "Process Development Kits" for Foundry customers in the Analog & Mixed Signal space,
    b. delivering computational lithography solutions for all technologies 45nm & above
    c. actively engaged in the development and characterization of 32/22nm technologies through explaining the physics of devices & materials, developing models to accurately predict electrical behaviour and debugging in realtime the electrical measurements from the fab to mature the process..

This is pioneering work in the industry in India and a demonstration that the computation intensive aspects of Semiconductor Process Development can be effectively done from remote geographies.

2) ASICs & IP – this department is responsible for :
    a. ASIC Design Center : end to end engagement on 65/45nm technology based SoCs for customers world wide. The team has delivered 20+ SoCs and impacted LTR of $800 Million +. This team has been instrumental in winning confidence and repeat orders form some very tough customers
    b. IP Development : The team has established competency in delivering complete cores for High Speed Links, I/O cells and Memory blocks besides the completing porting and characterization of IP libraries.
3) Processor Development -- In a short span of two years this dept. has become a center of competency for Physical Design of the complex POWER and zGryphon technologies. It is building deep micro-architecture competency driving Unit level integration and verification.
4) Systems Engineering – This dept. has established a complete characterisation Lab for the POWER systems – the first such lab outside USA) and is driving system validation and characterization for 2U/4U systems. It is also responsible for Validation and characterization tool development.
5) EDA : This team is actively supporting the Design teams across India and China and developing back-end and front-end design automation tools.

These 3 years were a period of extensive growth and transformation for this LAB and it is now being recognized as a Globally Competitive LAB critical to the success of the Technology and Microelectronics business. It is now headed by an International Assignee and has grown to 800+.

Since July 2012, I was leading an organizational initiative around technical vitality across the 2000+ Systems & Technology lab, extending this to the 100,000+ IBM India technical community.

Nov. 1999 to May 2007: TEXAS INSTRUMENTS BANGALORE -

Sept. 2005 to May 2007 : **Director, Strategic Programs**,. I worked on 3 different areas :

1. Worked with the RFID and medical Electronics Business Units on the strategy for business development to support India market and initiating product development at TI-India
   - Charted out the India Market Landscape and revenue projections and proposed a business development strategy. Established the sales and distribution channel and worked towards implementing this strategy by building an eco-system of partners and customer support model.
   - Formed a consortium of 17 companies who are key players in the RFID space in India to launch a Market Survey in India. Initiated conversion of this to the RFID Society of India .
   - Represented TI in Core Team for FICCI- Medical Electronics Forum
   - Secured the first RFID Sales Deal of $1.5Million per year. Business plan for 2007 $2Milllion +.
2. Worked with the Sales & Marketing organization to establish the right support model for the Multinational Design Houses in India
   - Surveyed the Mutlinationals in India and mapped them to the Top Accounts for TI
   - Focused of top 3-5 accounts to pilot a concept of a Virtual Support Model - leveraging the R&D, Tech Support and Sales Teams at TI-India alongside the World-wide account Sales & Marketing and Business Development Organisations Displaced incumbent at a key VoIP account to secure $5Million sales for TI.
3. Sales & Marketing Support by Account management of key Telecom Accounts. First $ 1 Million account

2003 to 2005: **Director, Cellular Systems SW R&D.** I had the primary role in capturing a $2.5Billion low cost cell-phone chipset market opportunity, by establishing a 200+ SW Organisation for the Cellular Systems Business of TI. I performed the following functions:

1. Defining Strategy, Work Partitioning, Working Model, Orgn. Structure and ramp-up of a 140+ member team focused on Modem SW development. The strategy revolved around the twin objectives of:
   - leveraging the presence in this region to develop and support products targeted for this region
   - leveraging the presence of SW competencies available in India (directly and through 3rd parties)
2. Integrating the OMAP* SW development team (70+) into the Cellular Systems SW and SWCOE* Framework
3. Extending the Solution Delivery (15+) activity to provide support on the Modem as well as Multimedia platforms to customers in the Asia Pacific region (Japan, Korea, China, Taiwan)
4. Initiating the Program Management, CTO & Business Development activities towards building a holistic organisation and driving the Low-Cost Product-line in the most cost-effective manner.

The key accomplishments of the teams were:

- Complete SW delivery on the single chip cell-phone, reference platform. Setting industry standards in achieving a voice call in 14 days after first silicon samples, leading to more than 7 customer design-ins. This was accomplished by a new team within 15 months of ramp-up. This resulted in $2.5 billion revenues for 2 subsequent years.
- Over 10 OMAP design wins, through Solution Delivery activities.
- Establishment of complete System Test Lab resulting in ~$1.5 million savings from external test houses and regular 6 week releases of customers.
- On-time and quality releases of Platform support packages and MMI (Man-machine Interface) subsystem for all cellular systems platforms.
- Successful CMMI-L3 assessment for all teams

2001 to 2003: **General Manager, Broadband Applications**. My primary role was to work with the Business Units in the TI-BCG(Broadband Communication Group) Organisation to establish and operate an 85 member BCG-SW organisation consisting of Cable, DSL, VoIP & SPTC teams in TII-SWCOE*. I performed the following functions:

1. Defining long term charter and organization structure for each of the teams and ramping up teams with the appropriate experience profile.
2. Establishing the effective work partitioning and working model for each of the teams within the world-wide organization and the SWCOE
3. Establishing & tracking priorities for the teams & the management of the SW engineering process framework for successful execution of projects.

The key accomplishments of the teams have been:

1. Cable: A team of 10-20 members has established TI as the industry leader in the Voice over Cable space. This has now become the core of TI's Competitive Strategy in the Cable Market. TI's PacketCable solution on ARRIS and TOSHIBA platforms was the only one to get certified in 2002. This team had complete ownership from Standards to Certification as well as Marketing & customer support (SAMSUNG, Toshiba, Arris and Tellabs). The team effectively worked with TI-Germantown and TI-Israel to integrate the Golden Gateway and TI-DOCSIS sub-systems into the PacketCable offering.
2. DSL: A team of 26 members executed the ANNEX-C of ADSL (targeted for the Japan market) on TI's CO and CPE Platforms. The team also successfully developed the Real-time subsystem for the ADSL+ and ADSL2 solutions. The team road mapped and prototyped the DMS (DSL Management System) as a debug-diagnostic tool for TI's CO and CPE solutions. The team generated several patents and contributing standards in the ADSL-SELT (Singe Ended Loop Test) and Annex-C areas.
3. VoP : A team of 34 members was responsible for the C55X offering on TI's VoP platforms for CPE and Infrastructure. The team has been delivering best-in-class, wireline and wireless speech codec components on TI platforms. The team also delivered the 192 voice channel and 90 modem channel build on the Janus Platform. The team is responsible for C64X VoP solutions and feature enhancements for the IP-Phone (e.g. MP3 integration) and High Density Voice (e.g. Tandem Free operation) Platforms.
4. SPTC*: A 14 member team in India has been responsible for VxWorks, Linux (also Nucleus and WinCE) Platforms for TI's BCG* platforms.

1999 to 2001 : **Program Manager, Cable Broadband Communications**. My role was to establish priorities & track the project execution for the 35 member CBC India team consisting of VLSI designers in the DSP orgn, analog designers in the MSP orgn. and system SW engineers reporting to me. The key accomplishments were:

- Bringing the Analog and VLSI engineers together with the CBC-Israel Team for the successful execution of TNET4042 (single chip CABLE Modem) TI's first and most complex mixed-signal SoC
- Ramping up of the Packet Cable team.

1998 to 1999 : Design Manager, Networking Products, Alliance Semiconductor, Bangalore. My primary role was to work with the Marketing Group and specify the product line which leverages the organisation's core competencies in memory technologies. I have performed the following functions :

1. Studied the performance bottle-necks related to end to end transport of TCP/IP packets through the Internet and architected out solutions for the look-up tables related to the L2/L3 and L4 Header Processing to facilitate wire-speed routing and packet classification & scheduling for QoS

requirements.
2. An innovative approach using specialised memories was adopted. This represents a breakthrough in memory technologies and offers simple and natural solutions for the "Hard-Problems" of "Longest Prefix Match", "Range Match" and "Multi-Dimension Filtering". Patents have been filed for these.
3. Defined a chipset of 5 devices. Detailed specifications were worked out and Verilog Behavioral models were developed which were delivered to potential customers.
4. 3 of these devices were implemented using 0.25 and 0.18 micron technologies. I was actively involved coordinating and reviewing the front-end and back-end design of these devices.
5. I was also been responsible for modifying the existing product-design cycle (followed by memory products) for the Networking Products. The emphasis here has been on automating layouts and combining the ASIC and Full-custom methodologies to have exhaustive functional and timing verification.

A team of 3 project leaders, 12 design engineers and 3 layout engineers has been directly reporting to me. In addition to this I have been involved in the establishment of the 50+ Bangalore Design Centre as a part of the management team of 4 people.

1996 to 1998 : Executive Director, Network Programs (NPI), Bangalore, India.

Starting from my home I had NPI Bangalore operations set-up in a Business Centre in a month's time. In 2 months time we were a team of 20+ engineers and 2 technical support people. The following projects were handled by this team :

1. Pair-Span Project: 2, 4 and 8 line "pairgain" systems using ISDN and HDSL interfaces. Complete design of 2 line system. Preliminary design of 4 and 8 line systems.
2. S Star Project: 16 x 16 ATM Switch Server using 155 Mbps links. 70% of the execution carried out at Bangalore. Server/Line Interface module (including a 3-way ATM switch FPGA of 30K gates) designed & developed and System Software Architecture defined in Bangalore.
3. Full Service Network Project: This project demonstrates end-to-end MPEG2 Video Delivery using ADSL to the customer premises. Prototyping, System Integration and Field Installations in China and Japan of the Distribution Element handled by Bangalore team.
4. Hotel Video System: This project demonstrates Interactive-TV with web browser and Video-on Demand Applications over coax cable for a hotel environment. The Bangalore team has been involved in the development of the Communication server and the Digital Video Server (MPEG2 to Video) for the Head-end System.

Besides setting-up these teams, my role also included day-to-day technical management and coordination with the US and NOIDA locations.

1989 to 1996: CDOT, Bangalore, India -

1996: Visiting Consultant at Network Programs, Piscataway NJ USA. During this 6 month period I handled 2 projects:

1. Virtual Private Networks' Service management : This service management application was intended to interface with the N/W management S/W of the customer and provide a distributed OSS platform. Generated User Requirements and translated them into Functional Specifications and Architecture Design -using a Client-Server model. I also generated the Test Specifications.
2. Distributed Network Management of an ATM over SONET Network : Generated the Test Plan and Specifications and performed the Integration testing of this Network Management Application.

1993 to 1996: Program Manager, Parallel Processing Group. I managed a group of 5 hardware engineers, 3 applications software engineers, 2 system software engineers, and 3 support personnel. The main activities of the group have been:

1. System integration and installation of the 192 node parallel processing system at the Indian Institute of Tropical Meteorology.
2. Support to 4 field installations of the 16 node and 64 node systems
3. Project proposals to Govt. Funding agencies for Parallel Processing Systems targeted towards real-time database search applications. Report to High Performance Computing Committee on Analysis of Processor Architectures for real-time and non real-time compute intensive applications.
4. Re-architecting and Technology upgradation of the system :
   - SuperSPARC based processing elements with 100Mbps communication links
   - Interconnection network based on GaAs crosspoint switch .

1989 to 1992: Research Engineer, Switching Division.

1. Design, Prototyping and Integration of the Memory Sub-system for the processor complex of C-DOT's Digital Switching System (DSS); resulting in a performance improvement from 6,500 BHCA to 24,000 BHCA and a cost reduction of Rs. 84,000 per base module.
2. Comparative Study of Switching System Architectures.
3. ASIC development for the Signaling Processor Unit in the CDOT-DSS, giving a cost reduction of Rs 50 per line. This ASIC was a First Time Success. This 30K gates 0.8 micron ASIC was the most complex ASIC developed at SCL till then and had the unique privilege of being the first ASIC to roll out of the SCL Foundry at SAS Nagar INDIA.
4. Comparison of ASIC technology vendors and CAD tools to support setting up the design environment for in-house, front-end design of ASICs.

1985 to 1988: Member of Technical Staff, AT&T Information Systems, Holmdel, NJ, USA.

1. Designed, developed and evaluated architectures for 32 bit microprocessors and their peripherals. I was the principal architect for the memory management unit of the AT\&T 32200 series chip-set. I also architected the Pre-fetch Unit for the first Pipelined Processor Implementation.
2. I was also involved in developing and integrating a UNIX-streams based device driver for a high speed parallel-bus based LAN which was to be used for networking AT\&T UNIX machines.

Industry Internships as a student :

1982 to 1983: Part-Time Apprentice, Uniscans \& Sonics Ltd., Chandigarh, India.
Designed and developed a Z-80 based intelligent, colour graphics terminal [Personal Computer].

1982 Summer: Summer Trainee, Uniscans & Sonics Ltd., Chandigarh, India
Interfaced a speech synthesiser [TMS 5100] with a microprocessor [INTEL 8085] and developed a talking clock.

1981 Summer: Summer Trainee, CSIO, Chandigarh, India.
Designed a keyboard/LCD display interface for INTEL 8085 and developed a digital clock on it.

1980 Winter: Trainee, Regional Computer Centre, Chandigarh, India.
Developed inventory management software in FORTRAN on DEC 2050 in the Tops 20 environment.

PATENTS

1. US patent - 7233597granted June 19 2007, “High Speed Parser” – Pamela Kumar, Cyril Chemparathy, Mohit Sharma
2. US Patent – 6839799 granted Jan 4 2005, “Method for prioritization of database entries” - Pamela Kumar, Mohit Sharma et al.
3. US patent – 6925706 granted Nov 30, 2004 “Multiplexer”– Mohit Sharma, Pamela Kumar.
4. USPTO Publication- 20030005210 Jan2,2003 “Intelligent CAM cell for CIDR Processor”- TD Reddy, Mohit Sharma, Pamela Kumar
5. Regn. No.: 38,686 Filed on March 18, 1999" A Search Cell To Be Used as a Building Block of a Database and Capable of Performing Heirarchical Search in the Database and The Method Thereof" - TD Reddy, Pamela Kumar, Bhanu V.R. Nanduri, Mohit Sharma, Saivakumar K. Kuttappan

3 patents filed on the “ IP routing accelarator”
2 Patents filed on “ Packet Classification engine”
2 patents filed on “ High Speed Parsing engine”
1 patent filed on “ Qos Scheduling”

PUBLICATIONS and PRESENTATIONS

1. “A Highly Testable ASIC for Telephone Signalling" Pamela Kumar, P.Jayalakshmi, S.Krishna Kumar, K.Ravishankar. Presented at The Eighth International Conference on VLSI Design, 1995.
2. “SuperSPARC based Processing Element for CHiPPS" Harikrishna C.Warrier, Pamela Kumar, B.S.Muralidhar, S.Selvakumar. Presented at The Third Conference on Advanced Computing, ADCOMP'95.
3. “Evaluation of RISC Processors for Realtime and High Performance Computing Systems" Pamela Kumar, Harikrishna C. Warrier, M.Periasamy. Manuscript submitted to review for publication as a book to Tata McGraw Hill, Narosa Publishing House and Allied Publishers Limited.
4. “Specialised Memory Architectures” Pamela Kumar, IEEE Bangalore Chapter Invited lecture – Sept. 1999
5. “DOCSIS Tutorial” Pamela Kumar –Commsphere2000, IIT-Madras Feb. 2000
6. “New TI Solutions drive deployment of VoIP over DSL and Cable” Pamela Kumar and Prakash Easwaran DSPFEST, Dec.2000
7. Student Projects :
   - “ MPLS implementation on TI’s Thunderbird platform” with Prof. Karandikar at IITB -2000
   - “ Encryption Algorithms on C55XX” with Prof. Vinay at IISc – 2001
   - “ Networking Accelarators” with IITKGP students - 2001
8. “Home Networking : Competing technologies for the last 100m” Pamela Kumar - DSPFEST, Dec 2002
9. “Enabling the Broadband Home Revolution” Pamela Kumar –Techfest2003, IIT Mumbai, Feb. 2003
10. “ Chip Design for Wireless Systems” Pamela Kumar -IETF Oct 2005
11. Panelist- RFID Workshop – IIT Kanpur, Nov. 2005
12. Keynote Address – RFID and Session Chair “ Emerging Technologies “ – TIDC-2006
13. “Wireless sensors for Personal Medical Devices”, International Conference on Medical Electronics”2006, FICCI
14. “RFID Usage in 2010 “ – BIG 2006, CSI Bangalore Chapter
15. “ Solutions for a Smarter Planet” Key Note - Dec 2009 IEEE Women in Technology Region 10 Conference
16. “ Technical Careers vs Management Careers” - May 2008 – Silicon India sponsored “Womens Day Conference”
17. Panelist on Cloud Computing panel organized by Zinnov Consulting – March 2011
18. “Emergence of the Intercloud” Standard for Intercloud Interoperability and Federation (SIIF) – 1st International Conference on Advanced Cloud Computing, Oct 2012
19. Lecture at IIMB, PGDM Class, Feb 2013 – “Corporate Entrepreneurship – 2 Case Studies”
20. Invited Speaker, SNIA India Information Infrastructure Conference, 2013 “ Cloud Computing Innovation Council”
21. Panelist, NASSCOM Infrastructure Management Summit 2013 **“**Optimizing infrastructure through virtualization”
22. Invited Speaker, International Conference on Cloud Computing (ACC 2013 by CSI) – “ Cloud Computing Innovation Council”
23. IEEE-CCEM 2013 – Panelist and release of “Cloud Computing Adoption and Innovation in India – An Approach to a Road-map Whitepaper v1.0”
24. IEEE Women in Engineering, Live Chat Video, Sept 2013
25. Invited Speaker, OpenStack Mini Conference @ Open Source India, 2013 by EFY
26. Panelist, 7th Cloud Computing & Big Data Conference 2013 by VirtueInsights
27. Invited Speaker/Panelist, “Consilience 2013-14: Conference on 'Legal Issues pertaining to Cloud Computing in India”
28. Keynote + Workshop - All India IEEE Computer Society Student Congress 2013 (AICSSC)
29. Panelist, IEEE International Conference on Advanced Networks and telecommunication Systems (IEEE ANTS 2013)
30. Keynote and Panel - 7th Cloud Computing & Big Data Conference by Virtue Insights, “The Business Value of Mobile Cloud Computing – Role of Telcos in the Cloudscape “ Dec 2013
31. Talk at IIMB, PGDM Class – “Cloud Computing” , Feb 2014
32. Keynote – India Cloud Week, Feb 2014 “Cloud Computing Standards & Interoperability - The Global Landscape & the INDIAN OPPORTUNITY”
33. Keynote – IEEE-RAECS, Mar.2014 “Cloud Computing Standards & Interoperability - The Global Landscape & the INDIAN OPPORTUNITY”
34. Presentation on CCICI to DeitY Cloud Computing Strategy Committee headed by Kiran Karnik, Oct 2014.
35. Keynote – Dr Dobbs Conference, Nov. 2014 “Cloud Computing Standards & Interoperability”
36. IEEE ANTS – Dec 2014,: Technology, Policy Challenges & Solutions to enable the Digital India Vision. Panel Chair.
37. IEEE ANTS 2015 – Panel Program Chair & Panel Moderator “ Make in India – Next Generation Telecom” – Dec 2015
38. Invited Talks – March, April 2015 on “Cloud Computing Standards & Interoperability” at IBM Research India and IIT-Guwahati
39. Panelist “Women in Business in India”, 2015 AIB (Academy of International Business) Annual Conference - June 28,2015
40. Inaugural Keynote – Cloud Computing India 2015 – Aug 6, 2015
41. Women’s Symposium Talk at Ericsson Sprint for Results : Management versus Technical Career (30 to 40 minutes) - How to make the choice and the "mantras for success" – Sept 14, 2015
42. IEEE SMARTTECH – “CLOUD COMPUTING – Lowering the Barriers to Make in India” – Sept 26, 2015
43. Keynote “CLOUD COMPUTING – Lowering the Barriers to Make in India”- “WIE SYMPOSIUM 2015 - Build.Empower.Inspire” Nov 8, 2015, IEEE India Council WIE-AG in association with IEEE Bangalore Section
44. Feature article in IEEE WIE Magazine – “Closing Circuits on a Global Cloud Computing Platform” – Dec, 2015 issue
45. VLSI Design Conference, Plenary Talk and Panel – “Business Case for a Women’s Paradigm for Next Generation Technology” – Kolkata, Jan 5, 2016
46. Industry-Academia Conclave, Keynote–“Cloud Computing & IoT - Key enablers for DIGITAL INDIA and SMART CITIES”- IIT Indore, Feb19, 2016
47. Women’s day Keynote – “ Technical vs Management Career” MS Ramaiah Institute of Technology, March 8,2016
48. ICCTAC, Bangalore – Keynote “Cloud Computing & IoT - Key enablers for DIGITAL INDIA and SMART CITIES”, March 10, 2016
49. Women’s Day Keynote – “ Victory for Women”, GSSS Institute of Engg and Technology for Women, Mysore, March 12, 2016
50. Panelist “IoT and Cloud Computing”, 9Th Cloud Computing and Big Data Conference, Lalit Ashok, Bangalore, March 17, 2016
51. Inaugural Session Speaker “ CCICI Overview”, CCICI-NIST Workshop, Taj Vivanta, June 6, 2016
52. Keynote -“ A Business Case for Women’s Paradigm for Next Gen Technology” – IEEE R10 SWYL Congress, Lalit Ashok, Aug 26, 2016
53. Keynote – ‘IoT for Smart Cities – An India Perspective” , - DVCON, Leela Palace, Bangalore, Sept 16, 2016

54. Keynote – “Cloud Computing and Internet of Things- Key enablers for Digital India & Smart Cities” Cloud Security Alliance APAC Congress- 23rd November, 2016
55. Panelist – Digital Matrix, CeBIT, Bangalore, Dec 8, 2016
56. Panelist – Women in Tech Leadership, Disruptive Tech & Innovation Summit, Vivanta by Taj, M.G.Road, Bengaluru - 20th December, 2016
57. Plenary Speaker – Cloud Computing – Key enabler for Digital India, Indian National Science Congress, Tirupati, Jan 5, 2017,
58. Moderator - COMSNETS Panel - Smart Cities: Delusions of Grandeur? - Jan 7, 2017
59. Keynote – “Cloud Computing and Internet of Things- Key enablers for Digital India & Smart Cities” 30th International Conference on VLSI Design & 16thInternational Conference on Embedded Systems (VLSID2017). Hyderabad, January 10th 2017.
60. Keynote- “WOMEN’s PARADIGM in the Next Era of Science and Technology”, WiSE 2017 @ CeNSE, Jan 12, 2017
61. Moderator – Round Table on “ Cloud Computing for Banks” IBEX India 2017 I MMRDA Grounds, BKC, Mumbai, 20 January 2017
62. Panelist - Fidelity Career Trade Show – Fidelity Investments, Jan 23rd, 2017
63. Keynote & Panel Moderator-"Cloud Computing the Backbone of Digital India-Role of Standards & Interoperability" OPEN GROUP Conference, Bangalore, Feb 9, 2017

Professional Bodies:
Founding Chair & Vice President, Cloud-Computing Innovation Council of India.
IEEE Region 10 – Industry Relations Chair
IEEE ANTS 2016 General Co-Chair, Panel Chair – IEEE–ANTS (2013 to present)
Member IEEE Charles Steinmetz Awards Committee
IEEE Standards Association – Board of Governors – Member at Large from India (from Jan 2011) – driving the India Strategy for adoption of Standards and enhanced participation in development of Standards, Interfacing with the Cloud Computing Initiative to drive the development of Cloud Computing related standards. Liason to IEEE-Women in Engineering
IEEE Computer Society, Bangalore Chapter – Chair (2010 - 2012).Steered the Society from technical talks focus to technical workshops for professionals and students.
IEEE Bangalore Section- Executive Committee – Vice Chair (2017), Chapter Coordination and Membership Development(2009)
Medical Electronics Forum, FICCI - Founding member representing Texas Instruments.
RFID Industry Consortium – Coordinator. Formed a 17 company consortium - TI, IBM, Motorola, TCS, WIPRO, Cognizant, EPC, Gemini Communication, Muehlbaer, APK-ID, Syrmatech etc.). Drove the Indian ecosystem / market study leveraging Frost & Sullivan.
India Semiconductor Association – IBM representative
Member of TII Foundation; Active Blood Donor, Awards in State level & National Level Public Speaking Contests

Hobbies : Vocal Music, Cycling, Trekking, Cooking, Yoga and Naturopathy

DETAILS OF SOME DEVELOPMENT PROJECTS (in reverse chronological order)

1. **Definition of Alliance's Networking Products :** The chipset defined and architected to address the Header processing of TCP/IP packets consists of :
   - **ARP-L2:** 32k x 128 BINARY CAM Address Resolution Processor(Layer 2) with Global Mask Registers and address based prioritization to resolve multiple matches. Lock and Hit features to support replacement algorithms and next match detection for alternate routing. Designed for 100 Mhz , 3 cycle pipelined operation in 0.18 micron technology.
   - **IPRP-V4:** 64K X 32 specialised Logic-CAM based IP Routing Processor (Layer 3) capable of performing Longest Prefix Match (for an IP ADDRESS ROUTING table based on CIDR Protocol). Performs atomic updates and does not require presorting of tables. Prototyped and tested using 0.25 micron technology for 66Mhz, 2 cycle pipelined operation.
   - **IPCE-V4:** 16K X 112 Internet Packet Classification engine (Layer 4) performing 5 dimension filtering with 2 dimensions for prefix match, 2 for range match and 1 for exact match. This also features atomic updates and distributed prioritization to resolve mutiple matches ; requiring no pre-sorting of tables. This has been designed for 0.18 micron technology and 66Mhz, 3-12 cycle pipeline (depending on levels of priority).
   - **NIFD:** This device provides a UTOPIA interface for the data path and PCI interface for the control path for the ARP, IPRP and IPCE devices. It features a parsing engine which facilitates look-up based on Layer 2 to Application layer header information. It also allows the construction of complex look-up tables using a combination of ARP, IPRP and IPCE devices. Preliminary specification has been worked out.
   - **QoSS:** This device uses the Packet classification information to store and schedule packets at the output buffer queue. It facilitates implementation of various scheduling algorithms. Preliminary specifications worked out.

   The Product Design Cycle for these products was worked out as follows :

a) The QUAD design consisting of specialised Cells and word structures has been done using full-custom schematics (combination of CMOS and Dynamic logic) and layout. Verilog Netlist for this was generated using Switch level Modelling to facilitate functional verification.
b) The Control Logic and Data Paths have been designed using Verilog and synthesised using 0.25 micron STD Cell libraries. STATE CAD has been used for the State Machine design. Layout has been done using Silicon Ensemble.
c) Diva LPE is being used for the parasitic extraction and speed path Spice simulations and to back annotate timing information into the Verilog Netlist.
d) Power bus modeling is to be done to verify the suitability of the power bussing . Coupling guidelines have been determined and implemented to maximize noise margins. Low power techniques have also been implemented wherever appropriate.
e) Production qualification Test vectors (based on single stuck-at fault model) are also being used for final Functional/ Timing Verification.

2. Design of the Line Processing Module for the S* Project (ATM Switch/Server) : This Module provides the interface for a PCI-bus based server and a 155Mbps ATM over STM1 link to a 16 x 16 ATM switch. It also provides switching between the Server and the link with a broadcast provision. Further, it provides on-line snooping and transformation (i.e programmability based on VPI/VCI) of the ATM cells.

This design has been completed and includes a 30K gate FPGA implementing the 3-way switch, having UTOPIA 1 and UTOPIA 2 interfaces.

3. Prototyping , Deployment and Up-gradation of Distribution Element of the FSN System : The Distribution Element is an ATM Switch based Mux/Demux handling STM1 links (carrying MPEG2 over ATM) from the network side and ADSL or ATM25 links towards the subscribers.

- Taking over from the point where the PCB's were being manufactured and the design team had quit, an engineer and i stepped in and completed the prototype testing and rework and had the test set-up in place for delivery and installation of 12 Systems (over 100 cards of 5 card types) for deployment in China and Japan.
- Appropriate documentation and field trial support was also provided. All of this was accomplished in a period of three months.
- A feasibility study for up-gradation of the system to minimise cost per link has also been done.

4. **Communication Controller and MPEG2 Decoder for Head End of Hotel Video System Project :**

- The Communication Controller provides a 1Mbps communication link between the Head-End and the Set-top boxes (Guest Appliances) using the 0-70 Mhz bandwidth of the coax cable. This Controller card has been designed as an ISA bus PC add-on based on ELAN (a 486-based micro controller).
- The MPEG2 to Video decoder for 4 channels is also being designed as a PC add-on with a PCI bus interface.

5. **Technology up-gradation of the C-DOT parallel processing system:-**
   - **(a)** Performance study of the system to identify the impact of up-gradation of various subunits on the overall system performance.
   - **(b)** Exhaustive study and comparison of RISC processors for the selection of the processor for next generation of the system.
   - **(c)** The processing element (PE) was chosen to be the Super-SPARC or the DEC-Alpha. PE cards based on the SuperSPARC Processor were tested and integrated into the system. The 12 layer card housing 2 processing elements required only one iteration.
   - **(d)** Communication links were changed from 4Mbps HDLC links to 100Mbps FDDI links. The interconnection unit has been designed around a GaAs 16X16 cross-point switch capable of handling 1Gbps links was tested.

The team of engineers I was leading were all fresh BE's and hence required considerable guidance in their work.

6. **Set-up of ASIC Design Environment:-** This involved detailed study and comparison of ASIC Technology Vendors from the point of view of technology options, commercial aspects and customer support. Porting their Design Kits in the Dazix Environment and benchmarking them. A similar process of study, comparison and benchmarking of CAD Tool vendors was also done.

7. **ASIC Implementation of Signaling Processor for C-DOT DSS: -** This involved
- enhancing the functionality of the existing design to take care of field related problems and for improving testability.
- study of various partitioning options and choosing the optimal partition from the point of view of available technology and minimizing cost; also negotiating with various vendors for the best option.
- drawing up the test specifications for Functional Verification and ASIC testing for 95\% fault coverage.
- implementation of the ASIC using 1.2 micron gate array (30,000 gates) technology offered by Semiconductor Complex Ltd, India,. The design was done using Mentor Graphics tools. 94\% fault coverage was achieved and 96\% gate utilisation was achieved for the 2 layer metal, channeled gate array .
- the ASIC has been successfully validated in all versions of C-DOT switches as a First Time Success. It has gone into bulk production and was the first ASIC to rollout of the 0.8 micron SCL foundry at SAS Nagar (55% yield).
- this ASIC was used to evolve the ASIC technology vendor selection process in C-DOT.

8. Study of Digital Switching Systems:-A comparative study of the switching-fabric architecture of various digital switching systems was done emphasizing modular expansion, reliability features, maintainability features, overload handling etc.

9. **Design, Prototyping and Integration of the Memory Sub-system for the Processor Complex of the C-DOT DSS:-**The objective of this design was cost reduction by using 1 MB or 4 MB DRAM Modules and also to optimize performance (for BHCA improvement). A totally top-down approach was taken for the design involving the following steps --

(a) Architectural Study and Analysis was done to evaluate various options : Dram Access Modes, Dram Controller Design Options, Error Checking in Data Path - Hamming Code vs. Parity checking
(b) Based on these studies and the system level requirements the architecture and implementation were finalised.
(c) Detailed Timing analysis, Testability analysis and Fault Coverage analysis was done.
(d) Layout and Placement guidelines were evolved based on the study of cross-talk and ground bounce effects, decoupling requirements, termination requirements based on loading and transmission line effects. The card was finally routed on a 6 layer PCB.
(e) Prototyping was done using a MICE and subjecting the system to Functional, Parametric and Dynamic tests. Then the Hardware/Software Integration was done.
(f) Based on the results of the above steps and manufacturability considerations a production version of the card was made and integrated into the system.
(g) Detailed documentation for the design was done.

The card finally achieved almost 4 times performance improvement and Rs. 84,000 cost reduction.
The card design cycle was standardised using this card.

10. **Architectural Analysis of Sabre Processor:-** Behavioral Modelling and Analysis of the Pre-fetch Unit of a pipelined Processor to optimise the Instruction Cache Organisation, Branch Prediction Strategies & Pre-fetch Algorithms.

11. **Architectural Specification for 32201 MMU: -** This involved the following steps **--**
- comparative study of MMU's for 32 - bit processors
- analysis and finalizing of MMU features after extensive interaction with potential users
- address trace analysis to finalize organisation of Translation Look-aside Buffer (TLB) and Data Cache.
- study and evaluation of Technology options for implementation.

12. I/O Specifications for the CRISP Processor:-A detailed document on the pin-out, protocol and Timing diagrams was generated for the CRISP processor.

13. Design & Development of Z-80 Based Personal Computer :- Designed, developed and integrated the following
- Processor card with keyboard interface and a DRAM-based Memory card
- Video Controller card (using discrete logic) interfacing to a RGB monitor and a Video RAM-card
- Communication interface card with an I/O port based communication and a joystick interface

The software developed included --
- The Basic monitor program including --DRAM refreshing, keyboard, joystick and communication interface drivers, Video RAM and controller interface.
- The Graphics software included a library for Line drawing, rectangle drawing, pattern generator, character and graphics mixing, zooming and rotation of characters etc.