Exam.Code:0934
Sub. Code: 33755

2056

B.E. (Electrical and Electronics Engineering)

Fourth Semester

PC-EE-404: Microprocessor and Microcontroller

Time allowed: 3 Hours Max. Marks: 50

NOTE: *Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Unit.*

x-x-x

I. Attempt the following:-

(a) How many input devices can 8085 support and why?

(b) Differentiate between instruction cycle and machine cycle?

(c) What is the function of Ready pin ?

(d) Discuss function of Data Pointer in 8051?

(e) Differentiate the instructions LDA and LDAX. (5x2)

UNIT - I

II. (a) WAP to count continuously in hexadecimal from FFH to 00H in a system with 0.5 μs Clock period. Use Register C to set up a one millisec delay between each count and display numbers at one of the output ports.

(b) Draw timing diagram of the instruction :

2058H MVI D 65H

If the clock frequency is 6 MHz, how much time is taken by the above instruction for execution. (6,4)

III. (a) A set of eight data bytes is stored in the memory location starting at XX50H. Check each data byte for bits D_0 and D_7. If D_0 or D_7 is 1, reject the data byte: otherwise store the data bytes at memory location starting at XX60H

(b) Discuss the Addressing Modes of 8085 quoting examples from the above program. (6,4)

P.T.O.

IV. (a) Draw timing diagram of instruction RET in 8085.

(b) Design a schematic for interfacing a memory IC 2764 (8K x8) with 8085. Using a 74LS138 (3 to 8 decoder) ,thereby generating address range for the Memory IC 8000H to 9FFFH . (4,6)

UNIT - II

V. (a) Give block diagram of Programmable Peripheral interface 8255.

(b) Discuss 8051 memory. (5,5)

VI. (a) Discuss the Interrupts in 8085.

(b) Explain interfacing of a common cathode seven segment display with 8085. (5,5)

VII. Write short notes on any three of the following :

(a) Interrupt Priority in 8085

(b) Programming Model of 8085

(c) Partial decoding vs Absolute decoding

(d) Tri-state logic (4,3,3)

x-x-x