Exam. Code: 0916
Sub. Code: 33433

2056

B.E. (Computer Science and Engineering)

Fourth Semester

CS-405: Computer Architecture & Organization

Time allowed: 3 Hours **Max. Marks: 50**

NOTE: ***Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Section.***

x-x-x

Q 1. (a) Draw and explain the connections between processor and memory. **[5 x 2 = 10]**
(b) Write or draw the steps to execute an instruction that loads a number from memory location to processor register. State assumptions clearly.
(c) Draw the Add/Subtraction algorithm for sign-magnitude data.
(d) Which parameters influence the choice of page size in virtual memory systems?
(e) State and briefly explain the pipeline hazards.

SECTION – A

Q 2. (a) Draw and explain 8085 microprocessor architecture. [5]
(b) Explain various addressing modes with the help of examples. [5]

Q 3. (a) Write a program to perform sorting of numbers using bubble sort algorithm. State your assumptions clearly and explain your solution with the help of an example. [5]
(b) What is instruction set completeness? Validate the same by listing a complete instruction set.[5]

Q 4. (a) Draw and explain the flowchart for the following: [6]
i) 2's complement addition/subtraction algorithm flowchart with example
ii) 2's complement multiplication algorithm flowchart with example
(b) Compare hardwired and microprogrammed control units. [4]

SECTION – B

Q 5. (a) Draw and explain synchronous DRAM. Also, explain its burst mode with the help of an example. [5]
(b) A block – set – associative cache consists of a total of 64 blocks divided into 4 – block sets. The main memory contains 4096 blocks, each consisting of 128 words.
i) How many bits are there in each of TAG, SET and WORD fields? [3]
ii) What will be the impact of increasing or decreasing size of cache blocks? Explain your answer with example. [2]

Q 6. (a) Write a note on virtual memory. [3]
(b) Draw and explain I/O interface circuit. Also state and explain two mechanisms that can be used for synchronizing data transfers. [2,5]

Q 7. (a) Explain instruction hazard in pipelining. Also state and explain various ways to remove or reduce the impact of hazard. [6]
(b) Write a note on Interrupt driven I/O. [4]

x-x-x