Exam.Code:0976
Sub. Code: 34653

2056

M.Tech (Microelectronics)

Second Semester

MIC-204: Advanced Memory Technology & Design

Time allowed: 3 Hours **Max. Marks: 50**

NOTE: Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Part.

x-x-x

Q1) a) What are peripheral circuits in a memory chip? List any three. (2)

b) What is the row hammer effect in DRAM and why is it a security concern? (2)

c) What is the difference between auto-refresh and self-refresh in DRAM? (2)

d) Differentiate between NMOS and CMOS memory cell circuits in terms of power and noise margin. (2)

e) What is a Half-VDD generator and why is bit-line precharge to VDD/2 preferred? (2)

PART -A

Q2) a) Explain the I/O interface design of a memory chip. How does the I/O interface handle signal integrity issues such as SSO noise and termination? (5)

b) Describe the design of a sense amplifier for SRAM and DRAM. Explain the latch-type sense amplifier and derive its regeneration time constant. (5)

Q3) a) Explain working of CMOS transmission gate and how it is used in pass-transistor-based memory. Compare 6T SRAM with 4T and 5T variants in terms of area and stability. (5)

b) Explain scaling laws for memory devices.What are the fundamental limits of DRAM and SRAM scaling? (5)

Q4) a) Describe the design and operation of Dickson charge pump with N stages. (5)

b) Explain the basic operation of a DRAM memory cell during read and write cycles. Describe the charge-sharing phenomenon, derive the voltage change on the bit line, and explain why the read is destructive. (5)

P.T.O.

PART -B

Q5) a) Describe the architecture of a high-performance DRAM chip with emphasis on pipelined read/write operations. (5)

b) Explain DRAM redundancy implementation in detail. Describe how a row redundancy circuit works at the circuit level including fuse array, address comparator, and spare row decoder. (5)

Q6) a) Describe the hierarchical memory system in a modern computing platform. Explain cache memory organisation (direct-mapped, set-associative, fully associative) and inclusion/exclusion policies. How does the memory subsystem affect performance through AMAT? (5)

b) Explain DRAM addressing with multiplexed RAS/CAS architecture. How does DDR5 differ from DDR4 in its command/address bus structure? (5)

Q7) a) Describe the architecture of an on-chip refresh controller including refresh counter, timing generator, and interaction with normal operations. (5)

b) Describe the evolution and technology of embedded DRAM (eDRAM) for on-chip memory applications. Compare eDRAM with conventional SRAM for last-level cache. (5)

x-x-x