Exam.Code:0976
Sub. Code: 34652

2056

M. Tech. (Microelectronics)

Second Semester

MIC-203: Analog and Mixed Signals Device Design

Time allowed: 3 Hours **Max. Marks: 50**

NOTE: Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Part.

x-x-x

Q1) a) State one key advantage of a CMOS op-amp over a bipolar op-amp. (1)
b) What is an analog multiplier and what does it compute? (1)
c) In the 741 op-amp, what stage provides the high voltage gain? (1)
d) What is the significance of the unity-gain bandwidth (GBW) product in an op-amp? (1)
e) What does SPICE stand for in the context of circuit simulation? (1)
f) Briefly explain functionality of a source follower (common-drain) stage? (1)
g) In a common-source amplifier, what determines the voltage gain? (1)
h) What is the body effect in a MOS transistor? (1)
i) Why cascode current mirror it used? (1)
j) Define threshold voltage (V_{th}) of a MOSFET. (1)

PART -A

Q2) a) Derive the small-signal voltage gain, input resistance, and output resistance of a common-source amplifier with a source degeneration resistor Rs. Also discuss the effect of Rs on gain and linearity. (5)
b) Explain the concept of frequency response in a MOS amplifier. Derive the expression for the dominant pole frequency using the Miller approximation for the gate-drain capacitance C_{gd}. How does Miller effect limit bandwidth? (5)

Q3) a) Compare NMOS and CMOS inverter gain stages for use in analog VLSI. Derive the voltage transfer characteristic (VTC) and small-signal gain for a CMOS inverter operating in the saturation region. What is the advantage of the CMOS stage? (5)
b) Derive the output resistance of a cascode current mirror. Show mathematically why it provides significantly higher output resistance than a simple current mirror. Also discuss its limitation regarding output voltage headroom. (5)

Q4) a) A common-gate amplifier is biased with a current source at its source terminal. Derive expressions for voltage gain, input resistance, and output resistance. Under what conditions is the common-gate stage preferred over a common-source stage? (5)
b) Explain the design of a Widlar current source. Derive the relationship between the reference current I_{REF} and the output current I_{OUT} involving the degeneration resistor R_E. Why is it more suitable than a basic mirror for generating small currents from a large reference? (5)

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PART -B

Q5) a) Draw MOSFET-based circuit of Gilbert Cell, explain its operating principle, and derive the output current expression in terms of the two differential input voltages V_1 and V_2. (5)

b) Define slew rate of an op-amp and derive its expression for a two-stage CMOS op-amp with compensation capacitor C_C. Explain how slew rate limits large-signal sinusoidal output. (5)

Q6) a) Using a circuit diagram, explain the operation of a MOS differential amplifier under common-mode input and derive the common-mode gain A_{cm}. Show that a high-impedance tail current source suppresses common-mode signals." (5)

b) Explain the concept of input offset voltage and input bias current in an op-amp. How do device mismatches in a MOS differential pair contribute to offset voltage? (5)

Q7) a) Compare serial ADC and successive approximation ADC on the basis of speed, resolution, circuit complexity, and power consumption. Also list their applications. (5)

b) With a neat block diagram, explain the working of a 3-bit Flash ADC. Derive the number of comparators required for an N-bit flash ADC. Also state two major drawbacks of flash ADC. (5)

x-x-x