Exam.Code:0931
Sub. Code: 33690

2076

B.E. (Electronics and Communication Engineering)

Seventh Semester

Elective – IV

EC-704: Computer Architecture and Organization

Time allowed: 3 Hours Max. Marks: 50

NOTE: *Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Unit.*

x-x-x

I. Explain briefly the following:-

a) Design EX-OR gate using 4 NAND gates only.

b) How the throughput improve the efficiency of processor?

c) Detail the demerit of single address instructions.

d) Memory mapped I/O.

e) Code and Data Memory. (5x2)

UNIT - I

II. Design a 4-bit adder/subtracter circuit using full adders and explain its function. (10)

III. Discuss the factors influencing performance. Also, define addressing mode and explain the basic addressing modes with an example for each. (10)

IV. What is a data hazard? How do you overcome it? And discuss its side effects. (10)

UNIT - II

V. How the parallel port output interface circuit works? (10)

VI. What is a mapping function? What are the ways the cache can be mapped? (10)

VII. Explain synchronous DRAM technology in detail. Also explain, a cache-based memory system using FIFO for cache page replacement. (10)

x-x-x