Exam.Code:0929
Sub. Code: 33664

2076

B.E. (Electronics and Communication Engineering)

Fifth Semester

EC-501: VLSI Design

Time allowed: 3 Hours Max. Marks: 50

NOTE: Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Unit.

x-x-x

1. Attempt the following questions:-
   a) What is meant by "fan-out" of a CMOS gate?
   b) Define dynamic power dissipation in CMOS logic.
   c) What is a stick diagram and why is it useful before full layout?
   d) Distinguish between static CMOS logic and dynamic CMOS logic in one line each.
   e) What is "voltage scaling" in VLSI and why is it attractive for low-power design? (5x2)

UNIT - I

2. a) Explain why silicon is preferred over germanium as a substrate material for VLSI. Include discussion on bandgap, leakage, and thermal aspects.
   b) Describe, with a simple flow, how silicon wafers are prepared starting from a grown crystal ingot up to ready-to-use polished wafers. (2x5)

3. a) Discuss any two common crystal defects (e.g., dislocations, vacancies) and explain how such defects can affect device yield and performance in VLSI circuits.
   b) Explain the basic steps involved in thermal oxidation of silicon. Comment on how oxidation temperature and ambient (wet/dry) influence oxide thickness and quality. (2x5)

4. a) Describe the sequence of operations in a generic MOS process to form source and drain regions using ion implantation, including masking, implantation, and annealing.
   b) Compare plasma etching and wet chemical etching for pattern transfer of contact holes, 5 pointing out at least two reasons why plasma etching is preferred for submicron technologies. (2x5)

P.T.O.

UNIT - II

5. a) Starting from the gradual-channel approximation, write the drain current expression of an nMOS transistor in saturation and identify each parameter's physical meaning (mobility, oxide capacitance, W/L, overdrive voltage).

   b) Explain qualitatively how short-channel effects influence threshold voltage and drain current in deep submicron MOSFETs, mentioning drain-induced barrier lowering (DIBL) and velocity saturation. (2x5)

6. Consider a CMOS inverter where $V_{DD} = 2.5$ V. The nMOS and pMOS are sized such that the switching threshold is approximately at $V_M \approx 1.2$ V.

   a) Explain how the relative sizing of pMOS and nMOS transistors can be chosen to obtain a switching threshold close to mid-supply, and why this is desirable.

   b) Define low noise margin and high noise margin. Sketch a generic VTC and indicate how noise margins are read from it. Briefly discuss the effect of shifting V_M on these noise margins. (2x5)

7. a) Implement the function $Y = A \cdot \bar{B} + \bar{A} \cdot C$ using static CMOS logic. Draw the pull-up and pull-down networks and comment on series/parallel connections in each network.

   b) Explain the basic operation of a master–slave D flip-flop using transmission gates, clearly indicating when the master and slave latches are transparent and when they hold data. (2x5)