Exam.Code:0933
Sub. Code: 33744

2076

B.E. (Electrical and Electronics Engineering)

Third Semester

PC-EE-304: Digital Electronics

Time allowed: 3 Hours Max. Marks: 50

NOTE: *Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Unit.*

x-x-x

Q.1a) Why are NAND and NOR called **universal gates?**

b) What do you understand by 'race condition' in flip-flops? How it is eliminated?

c) Draw the logic diagram of a one to four line demultiplexer

d) What is tri-state logic?

e) Explain the difference between EPROM and EEPROM. (5×2)

UNIT - I

Q.2a) Implement the given function using NAND gates only. F(X, Y, Z) =m(0,6). (4)

b) Express the function F(A,B,C)=A'B+C' in minterm (canonical SOP) and maxterm (canonical POS) form. (3)

c) Implement 2 input NAND gate function y = (AB)' using a 2:1 MUX. (3)

Q.3a) Realize the expression (4)

F(W,X,Y,Z) = Σm(3,6,7,8,9,10,12) using a 8:1 multiplexer.

b) Design a 2-bit Carry Look-Ahead Adder. Show the implementation using basic logic gates. (3)

c) Explain the input and output characteristics of a TTL logic gate. (3)

Q.4a) Define a Register. Construct a shift register form RS flip-flops and explain their operation. (4)

b) Convert a D flip-flop into a T flip-flop. Draw the logic diagram and derive the conversion table. (3)

c) Minimize the following Boolean function including don't care conditions: (3)

F=Σm(1,3,7)+d(2,5,6)

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UNIT - II

Q.5a) Explain the working of dual slope A/D converter. Compare the dual slope ADC with successive approximation ADC. (6)

b) A 14-bit SAR ADC is clocked at 5 MHz. What is the maximum conversion rate in samples/second? (4)

Q.6a) Describe the programmable logic blocks used in CPLD. Explain how the interconnection matrix works. (6)

b) Compare Binary Weighted DAC and R-2R Ladder DAC. Why is the R-2R DAC preferred? (4)

Q.7a) Differentiate between PLA and PAL in terms of structure, flexibility, and performance. (6)

b) Mention the applications of DAC and ADC. (4)

x-x-x