Exam.Code:0999
Sub. Code: 34969

2076

M.E. (Computer Science and Engineering)

First Semester

Elective - II

CS-8109: Advanced Computer Architecture

(For UIET Only)

Time allowed: 3 Hours | Max. Marks: 50

NOTE: Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Unit.

x-x-x

I. Answer briefly the following:-

a) Define Amdahl's Law and explain its significance in parallel processing.

b) What are the main properties of an ideal interconnection network?

c) Differentiate between a Multiprocessor and a Multicomputer.

d) Distinguish between CISC and RISC processors.

e) What is cache coherence? Why is it required in shared-memory multiprocessors? (5x2)

UNIT - I

II. (a) Explain Flynn's taxonomy of parallel computers. Compare SIMD and MIMD architectures with suitable examples.

(b) A parallel program runs on 8 processors and achieves 5.6×speedup over serial execution.

i) Calculate the parallel efficiency.

ii) Find the serial fraction (f) using Amdahl's Law.

iii) What will be the maximum speed up if 32 processors are used? (5,5)

III. (a) What are the conditions of parallelism in programs? Explain data and resource dependencies.

(b) A parallel program has 80% of its execution time parallelizable. Calculate the maximum speed up on:

(i) 4 processors

(ii) 8 processors, using Amdahl's Law. Comment on the results. (5,5)

P.T.O.

IV. (a) Compare CISC, RISC, Superscalar, and VLIW processors with suitable diagrams wherever necessary.

(b) Define efficiency and utilization in parallel systems and describe how they are measured. (5,5)

UNIT - II

V. (a) A program consists of 40% sequential and 60% parallel code. Calculate the speedup and efficiency when executed on 2, 4, 8, and 16 processors.

(b) Explain the Snoopy Bus Protocol for maintaining cache coherence in shared-memory systems. (5,5)

VI. a) A program has IC = 2.0×10^9 instructions, CPI = 2.0. It must finish in 1.0 s. What clock frequency (in GHz) is needed?

b) Explain Routing in Omega Network.

c) Explain the CM-2 architecture.

d) Explain any one vector access Memory scheme in detail.

e) Bernstein Conditions (5x2)

VII. (a) Explain the need for Synchronization in parallel programming. Discuss Locks, Semaphores, and Monitors with suitable examples.

(b) Explain demand-driven execution mechanism. Compare it with control-driven execution. (5,5)

x-x-x