Exam.Code:0970
Sub. Code: 34555

2055

M.E. (Electronics and Communication Engineering)

Second Semester

ECE-1205: VLSI Design

Time allowed: 3 Hours **Max. Marks: 50**

NOTE: Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Part.

x-x-x

Q1. a) What are the different fabrication steps involved in CMOS technology? (2)
b) Explain the concept of threshold voltage roll-off in MOSFETs and its impact on circuit design. (2)
c) Differentiate between charge sharing and charge leakage in dynamic CMOS circuits (2)
d) How does clock jitter affect synchronous sequential circuits? (2)
e) Why is Electromigration a critical issue in VLSI interconnect design? (2)

PART -A

Q2. a) Derive the MOS capacitor's Capacitance-Voltage (C-V) characteristics and explain its significance in MOSFET modeling. (5)
b) Compare the fabrication techniques of SOI, P-Well, N-Well, and Twin-Tub processes in terms of doping profiles, parasitic effects, and performance trade-offs. (5)

Q3. a) Explain different CMOS circuit styles, including Static CMOS, Pseudo-NMOS, Dynamic CMOS, and CVSL. Discuss their performance metrics in terms of power, delay, and noise margin. (6)
b) How does charge sharing impact dynamic logic circuits? Suggest techniques to mitigate its effect. (4)

Q4. a) Derive the setup time and hold time constraints in a sequential circuit and explain how they impact pipeline design. (4)
b) Design a 4-bit Wallace tree multiplier and explain how its structure improves delay performance compared to conventional multipliers. (6)

PART -B

Q5. a) Explain Programmable Logic Arrays (PLA) and Field Programmable Gate Arrays (FPGA) and compare their suitability for different VLSI applications. (5)
b) Discuss the role of CAD tools in VLSI and explain the significance of Logic Synthesis and Place & Route (P&R) tools in the physical design flow. (5)

Q6. a) Explain the Floor planning problem in VLSI, including placement constraints, congestion issues, and area optimization techniques. (5)
b) Describe Clock Tree Synthesis (CTS) and discuss different clock distribution techniques such as H-tree, Mesh, and Spanning Tree methods. (5)

Q7. a) Explain Switch-Level Simulation in VLSI. Compare it with Gate-Level and Transistor-Level Simulations in terms of accuracy and computational complexity. (5)
b) Discuss Placement and Routing Algorithms used in VLSI design. Explain the min-cut placement approach with an example. (5)

x-x-x