Exam. Code: 0906
Sub. Code: 33297

2055
B.E., Second Semester
EC-203: Digital Design

Time allowed: 3 Hours **Max. Marks: 50**

NOTE: ***Attempt five questions in all, including Question No. 1 which is compulsory and selecting two questions from each Section.***

x-x-x

I.

a) (1) Convert $(65)_7$ to $(?)_5$
(2) Add $(23)_8$ and $(67)_8$.

b) Design XOR gate using NOR gates only.

c) Write excitation table of JK flip flop.

d) Define the following terms for D to A converters: Resolution and Linearity.

e) What do you mean by Noise Margin and Propagation delay in logic families?

[5×2=10]

SECTION A

II. (a) Convert the following function to POS form:
(1) F (A, B, C, D) = $\bar{C}D + AB\bar{C} + AB\bar{D} + \bar{A}\bar{B}D$
(2) Prove that (A+B) ($\bar{A}$+C) (B+C) = AC+B$\bar{A}$ **[3×2=6]**

(b) Implement full adder using half adders. **[4]**

III. (a) Minimize the following expression using K-map and implement the circuit using NAND gates only.
Y = Σm (2,3,4,5,13,15) + Σd (8,9,10,11) **[5]**

(b) Implement the following function using 4:1 MUX by taking A as input to MUX:
F(A, B, C) = Σm (0, 1, 3, 5, 6) **[5]**

IV. Convert SR flip flop to JK flip flop using excitation table. **[10]**

SECTION B

V. (a) How many bits are required for a D to A converter, so that its FSO is 12.6 V and resolution is 20 mV? **[4]**

(b) Explain 4-bit bidirectional shift register with the help of suitable block diagram. **[6]**

VI. (a) Design and explain two-input TTL NAND gate with the help of suitable circuit diagram. **[5]**

(b) Compare different Logic families on the basis of their performance characteristics. **[5]**

VII. Write note on following:
(a) Successive approximation type A to D converter. **[5]**
(b) Johnson Counter **[5]**

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