Exam. Code: 0906
Sub. Code: 33297

2015
B.E., Second Semester
EC-203: Digital Design

Time allowed: 3 Hours **Max. Marks: 50**

NOTE: ***Attempt five questions in all, including Question No. 1 (Section-A) which is compulsory and selecting two questions each from Section B-C.***

x-x-x

Q.No.	Section-A (All questions are compulsory)	Marks
1	a) State and prove De Morgan's theorem. b) What is the use of enable input in a decoder? c) What is the difference between a ring counter and a Johnson counter? d) What are the three possible output states of a tri-state IC? e) Why are voltage DACs are generally slower than current DACs?	10
	Section-B (Attempt any two questions)	
2	a) Obtain the minimal POS using Q.M method for function $\pi M(0,1,4,5,9,11,13,15,16,17,25,27,28,29,31).\pi d(20,21,22,30)$ and implement using minimum number of NOR gates only if normal and complementary inputs are available	5
	b) Design a SOP circuit that will generate an odd parity bit for a 4-bit input.	5
3	a) What is the inhibited condition in an S-R flip-flop? How it can be avoided using J-K flip-flop?	5
	b) List PLA table for a BCD to excess-3 code converter.	5
4	a) Convert D to T and J-K to S-R flip-flop.	5
	b) Design a combinational circuit that compares two 4-bit numbers to check if they are equal. The circuit output is equal to 1 if the two numbers are equal and zero otherwise.	5
	Section-C (Attempt any two questions)	
5	a) For what minimum value of propagation delay in each flip-flop will a 10-bit ripple counter skip a count when it is clocked at 10 MHz?	5
	b) What is the disadvantage in a weighted type DAC? How this circuit can be modified to overcome this disadvantage.	5
6	a) Design and implement a synchronous 3-bit up/down counter using J-K flip-flops. (If control M=0 down counting and M=1 up counting)	5
	b) Differentiate open collector and totem pole TTL. Explain how propagation delay is improved in totem pole TTL?	5
7	a) What are the characteristics of ECL family? Explain working of ECL circuit as an OR/NOR gate.	5
	b) What is a universal shift register? Explain working of a 4-bit universal shift register controlled by 4x1 multiplexers.	5

x-x-x