Exam.Code:0929
Sub. Code: 33664

2125

**B.E. (Electronics and Communication Engineering)**
**Fifth Semester**
**EC-501: VLSI Design**

**Time allowed: 3 Hours** **Max. Marks: 50**

***NOTE:*** ***Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Section. Use of scientific calculator is allowed.***

*x-x-x*

**Q1. Answer the following: -**

(a) Why accumulation region is not used in MOSFET conduction? (1)
(b) What is the condition on growth rate to avoid polycrystalline growth of epitaxial layer? (1)
(c) Which companies are called as Integrated Device Manufacturer? (1)
(d) What is the difference between dopant and carrier concentrations? (1)
(e) Why oxidation rate is faster in p-type than n-type silicon? (1)
(f) What is pre-deposition and drive-in phase during diffusion of dopants? (1)
(g) Why wet oxidation process is not preferred for gate oxide preparation? (1)
(h) How many different masks are used during CMOS fabrication process? (1)
(i) Why lower wavelength light is preferred in optical lithography? (1)
(j) Why anodic oxidation is not preferred for masking or gate oxide preparation? (1)

## SECTION A

**Q2.** (a) What is reaction limited and diffusion limited regime during the thermal oxidation process? (5)
(b) What is e- beam lithography and what are its advantages over optical lithography? (5)

**Q3.** (a) Derive the equation of maximum attainable pull rate in Czochralski process of crystal growth. (5)
(b) What is annealing and how it is important in ion implantation process? (5)

**Q4.** Derive the relation showing the dependence of rate of change of concentration of dopants with time in terms of diffusivity and concentration gradient during diffusion process. (10)

## SECTION B

**Q5.** (a) Design 1-bit full adder using transmission gate. (5)
(b) What is power dissipation? Derive relation for short circuit power dissipation (5)

**Q6.** (a) Calculate the threshold voltage $V_{To}$ at $V_{SB} = 0$, for a polysilicon gate n-channel MOS transistor, with the following parameters: substrate doping density $N_A = 10^{16}$ cm$^{-3}$, polysilicon gate doping density, $N_D = 2\text{x}10^{20}$ cm$^{-3}$, gate oxide thickness $t_{ox} = 500$ A$^0$, and oxide-interface fixed charge density $N_{ox} = 4\text{x}10^{10}$ cm$^{-2}$. ($n_i = 1.45 \text{ x } 10^{10}$ cm$^{-3}$, $\varepsilon_{ox} = 3.97\varepsilon_o$, contact potential = -0.9 V) (5)
(b) What are the five regions of operation of CMOS inverter, Discuss? (5)

**Q7.** Calculate $V_{OL}$, $V_{OH}$, $V_{IL}$, $V_{IH}$, $NM_L$, and $NM_H$ for a two-input NOR gate fabricated with CMOS technology. [$(W/L)_P = 8$, (W/L)n = 1, $V_{Tn} = 1$ V, $V_{Tn} = -1$ V, $\mu_n C_{ox} = 40\ \mu A/V^2$, $\mu_p C_{ox} = 20\ \mu A/V^2$, $V_{DD} = 5$V] (10)

*x-x-x*