Exam.Code:0921
Sub. Code: 33522

2125

B.E. (Information Technology)

Third Semester

PC-IT-302: Computer Architecture and Organization

Time allowed: 3 Hours

Max. Marks: 50

***NOTE**: Attempt <u>five</u> questions in all, including Question No. I which is compulsory and selecting two questions from each Unit.*

x-x-x

I. Answer the following briefly:-

(a) Explain processor-level data flow representation.

(b) What is the role of temporary registers in datapath design?

(c) Define microinstruction sequencing.

(d) What is a zero-address instruction?

(e) Define relative addressing.

(f) What is bus arbitration?

(g) What is cache write-back policy?

(h) Define associative memory search operation.

(i) What is structural hazard in pipeline?

(j) Define tightly-coupled multiprocessor. (10×1)

UNIT - I

II. Discuss the system design methodology and distinguish between gate-level, register-level, and processor-level design. (10)

III. a) Describe the phases of the instruction cycle with an appropriate example.

b) Illustrate the working of accumulator logic along with essential control signals. (2x5)

IV. Compare hardwired and microprogrammed control units, highlighting their merits and limitations. (10)

UNIT - II

V. Analyse the CPU organisation, covering ALU structure, register organisation, and addressing modes. (10)

VI. Describe the operation of DMA, the architecture of a DMA controller, and interrupt-driven I/O. (10)

VII. a) Outline cache mapping techniques with suitable examples.

b) Discuss multiprocessor interconnection structures. (2x5)

x-x-x