Exam.Code:0969
Sub. Code: 34528

2125

M.E. (Electronics and Communication Engineering)

First Semester

ECE-1104: Digital System Design

(For UIET Only)

Time allowed: 3 Hours | Max. Marks: 50

NOTE: *Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Unit.*

x-x-x

I. Attempt the following:-

a) Why commercial ECL families are not as popular as CMOS and TTL?

b) Define speed-power product. What is its significance?

c) Differentiate between latch and flip flops.

d) What are the types of memory?

e) Explain the DC noise margin of CMOS logic. (5x2)

UNIT - I

II. a) Why not use only non-inverting gates, so all signals are active high?

b) Give two examples of metastability that occur in everyday life. (10)

III. Discuss the process of converting a state diagram into logical circuit with the help of a suitable example. (10)

IV. Explain the different VHDL models used for simulation and synthesis of combinational circuits. (10)

UNIT - II

V. Discuss the procedure, how to find fault detection and location in sequential circuits. (10)

VI. Design positive edge triggered JK flip-flop and explain its functional and timing behaviour. Also write a VHDL program. (10)

VII. Explain the architecture of Built in self-test and discuss its operation briefly. (10)

x-x-x