Exam.Code:0922
Sub. Code: 6483

2054

B.E. (Information Technology)

Fourth Semester

PCIT-401: Microprocessor and Assembly Language Programming

Time allowed: 3 Hours Max. Marks: 50

NOTE: Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Unit.

x-x-x

I. Attempt the following:-

a) What is a Stack memory? Discuss LIFO and FIFO type of operation in stack register.

b) Which instruction of 8085 uses AC flag? Explain the instruction with an example.

c) Explain the operation performed when the following instructions are executed. How many bytes are consumed by them and which flag are affected by them?
CNZ, XTHL

d) Name Two instructions which have 6T-states for opcode fetch. Explain these instructions.

e) How many times the given loop will be executed? What will be the contents of HL register pair when the program control reaches to HLT instruction?

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MVI A, 00H
LXI H, 5003H
Loop: DCX H
DCR A
JNZ Loop
HLT
```

(5x2)

UNIT - I

II. a) What are the various Status flags provided in 8085? Discuss their role.

b) Explain the need to de-multiplex the bus AD_7-AD_0. How is the de-multiplexing done?

(2x5)

III. a) Write an assembly language program of 8085 to count the number of 1s and 0s present in hex byte at 9100h memory location. Store the number of 1s at 9101h and the number of 0s at 9102h.

Contd.....P/2

b) If a chip has addresses ranging from 2400H to 27FFH, then draw the hardware to generating logic low 'Chip select' signal that the processor will generate so as to select this chip. (2x5)

IV. Write a program to sort 10 bytes of data in ascending order. The data is stored at XX20H. (10)

UNIT - II

V. a) Write a set of instructions to cause a delay using register pair. Calculate the total delay caused if the register pair is loaded with A0F1H. Assume that the processor is running at 1Mhz.

b) Explain the working of IC 8255 with the help of a block diagram. (2x5)

VI. a) Write a subroutine to clear the flag register and accumulator.

b) Write a segment of program to exchange the contents of BC register pair with the DE register pair without using MOV instruction. (2x5)

VII. a) Differentiate between:-

i) Maskable and Non Maskable interrupts

ii) Level triggered- Edge triggered interrupts

b) Assuming that the microprocessor is completing RST 6.5 interrupt request, check to see if RST 7.5 is pending. If it is pending enable RST 7.5 without affecting other interrupts otherwise, return to the main program. (2x5)

x-x-x