Exam. Code: 0906
Sub. Code: 6258

2054

B.E. (Electronics and Communication Engineering)

Second Semester

EC-203: Digital Design

Time allowed: 3 Hours **Max. Marks: 50**

NOTE: ***Attempt five questions in all, including Question No. 1. which is compulsory and selecting two questions from each Part. Use of scientific calculator is allowed.***

x-x-x

I. **(a)** What is the difference between latch and flip flop? **(1)**

(b) List types of logic families. **(1)**

(c) What is meant by Mod of a counter? **(1)**

(d) What are the limitations of Karnaugh Map? **(1)**

(e) What is the difference between Synchronous and Asynchronous Counters? **(1)**

(f) What is weighted number system? **(1)**

(g) What is digital electronics? **(1)**

(h) What are drawbacks of weighted resistor D/A converters? **(1)**

(i) What are the differences between Combinational Circuits and Sequential Circuits? Give examples of each type. **(2)**

Part- A

II. **(a)** Explain full subtractor circuit. Implement it by using two 4:1 MUX only. **(5)**

(b) Convert JK flip-flop into D flip-flop. **(5)**

III. **(a)** Design a combinational circuit which has four inputs and one output such that the output is equal to 1 when:

(1) All the inputs are equal to 1

(2) None of the inputs are equal to 1

(3) An odd number of inputs are equal to 1.

Implement it by using single 4:1 MUX. **(5)**

(b) What are universal gates? Implement XOR and XNOR gates using NAND and NOR gates only. **(5)**

IV. **(a)** Simplify the following Boolean function using K-map into sum-of-products form and product-of-sums form. Implement each form using same type of logic gates.

$$f(A,B,C,D) = \sum(0,1,2,5,8,9,10)$$ **(8)**

(b) What is the largest binary number that can be expressed with 14 bits? What are the equivalent decimal and hexadecimal numbers? **(2)**

Part-B

V. **(a)** What do you mean by universal shift register? Explain the working of 4-bit shift register. **(5)**

(b) Design a 3-bit synchronous counter to count sequence 0, 1, 4 ,6, 7 and repeat using D flip flop. **(5)**

VI. **(a)** Sketch and explain the characteristics of CMOS inverter. **(5)**

(b) Explain the working of a dual-slope A/D converter with the help of logic diagram. **(5)**

VII. **(a)** A 6-bit-bit D/A converter has a voltage output of 0.8 V for a digital input of 100000. What can be the highest output voltage for the converter? **(3)**

(b) Define and explain the performance characteristics of D/A converters. **(4)**

(c) Define and explain the noise margin, propagation time and power dissipation of digital logic families. **(3)**

x-x-x