Exam.Code:0929
Sub. Code: 6597

2074

B.E. (Electronics and Communication Engineering)

Fifth Semester

EC-505: Digital System Design

Time allowed: 3 Hours **Max. Marks: 50**

NOTE: Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Part.

x-x-x

Q1

a) Explain difference between state reduction and assignment with the help of an example.
b) What is the minimum distance for a code in case of error detection?
c) Explain static hazard with example.
d) What type of codes are used in K-map designing and why?
e) What are prime implicants and essential prime implicants? (5 X 2=10)

Part A

Q2 Calculate the essential prime implicants for the following using Q-M method:
$Y = \sum m\ (0,5,6,8,9,10,11,16,20,24,25,26,27) + d\ (1,17,22)$
Also implement the circuit using NAND gates only. (10)

Q3 (a) Explain checksum and parity methods for errors occurred in digital data. (5)
(b) Design a combinational circuit which has four inputs and one output such that the output is equal to 1 when:
(i) All the inputs are equal to 1
(ii) None of the inputs are equal to 1
(iii) An odd number of inputs are equal to 1.
Implement it by using single 4:1 MUX. (5)

Q4 (a) Seven bit Hamming code 0010001 is received. Assume that even parity has been used. Check the error if any and find the correct code. (5)
(b) Explain path sensitizing method for fault detection in combinational circuits. (5)

Part B

Q5 (a) What are races? Explain cycles and hazards in asynchronous circuits. (5)
(b) What are Moore and Mealy machines? Compare the machines with the help of suitable circuit diagram. (5)

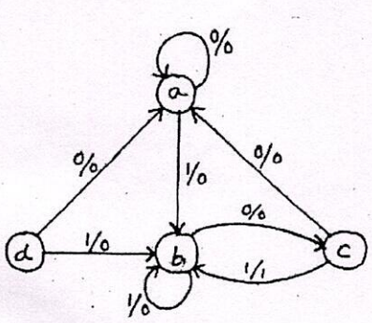
Q6 (a) Convert JK flip-flop to T flip-flop. (5)
(b) Derive the sequential circuit with two flip-flops A and B and one input x for the following conditions
(i) When x=1, the state of circuit remains same.
(ii) When x=0, then circuit through the state transitions from 00 to 01 to 11 and back to 00 and repeats. (5)

Q7 (a) Design a synchronous sequential machine for the following fault-detection experiment

Present State	Next State, Output Z	
	X = 0	X = 1
a	b,1	c,0
b	c,0	d,1
c	d,0	c,1
d	a,0	b,0

(5)

(b) Design a sequential circuit using T flip-flop for the following state diagram. Use state reduction if possible. (5)



x-x-x