Exam.Code:0929
Sub. Code: 6593

2074

B.E. (Electronics and Communication Engineering)
Fifth Semester
EC-501: VLSI Design

Time allowed: 3 Hours **Max. Marks: 50**

NOTE: ***Attempt five questions in all, including Question No. 1 which is compulsory and selecting two questions from each Section. All questions carry equal marks.***

x-x-x

1. Attempt all
   a) What is the body bias effect in MOSFET?
   b) What are the disadvantages of optical lithography?
   c) Compare isotropic and anisotropic etching process.
   d) What is symmetrical CMOS inverter?
   e) What are various types of diffusion?

Section A

2. (a) What are the factors that have led to the evolution and enhancement of VLSI Integrated Circuits?
   (b) Describe the various factors which must be taken into account in order to grow single crystals which are relatively free from defects in brief.
3. (a) Explain the different steps involved in n-well CMOS fabrication process with neat diagram.
   (b) Explain the formation of p-n junction. And, describe the variation of width of depletion layer under forward and reverse bias.
4. (a) Discuss the crystal refining process in detail. What are various defects?
   (b) Draw band diagram of PN junction under open circuit conditions and explain? What are the general specifications of PN junction diode?

Section B

5. (a) Explain the dynamic CMOS logic (Precharge – Evaluation) and discuss the cascading problem in dynamic CMOS logic.
   (b) Derive threshold voltage equation for short channel effect
6. (a) Explain the Short Channel Effects on threshold voltage and mobility of the charge carriers
   (b) Explain the MOSFET capacitances in detail
7. (a) What is voltage scaling and full-scaling in MOSFET?
   (b) What are the limitations of scaling in VLSI technology? Discuss the effect of any two limitations of scaling

x-x-x