Exam.Code:0933
Sub. Code: 6659

2074
B.E. (Electrical and Electronics Engineering)
Third Semester
PC-EE-304: Digital Electronics

Time allowed: 3 Hours **Max. Marks: 50**

NOTE: Attempt <u>five</u> questions in all, including Question No. I which is compulsory and selecting two questions from each Part. All questions carry equal marks.

x-x-x

Q1. (a) In 2's compliment representation, the number 11100101 represent which decimal number?

(b) Implement AND gate using XOR gates only.

(c) Give the performance characteristics of multiplexers.

(d) An 8-bit DAC has full scale output of 2mA and full scale error of 0.5%. If the input is 10000000, find the range of outputs?

(e) State the characteristics of semiconductor memories.

Part- A

Q2a. Solve using K-Maps:

$F(A,B,C,D,E) = M(1,2,6,12,14,26,29,30,31)$

b. Show how a full adder can be converted to a full subtractor with the addition of one inverter circuit.

Q3) Four large tanks at a chemical plant contains different liquids being heated. Liquid - level sensors are being used to detect whenever level in the tank A and B rises above a predetermined level. Temperature sensors in tanks C and D detect when the temperature in either of these tanks drops below a prescribed temperature limit. Assume that the liquid - level sensor outputs A and B are LOW when the level is satisfactory and HIGH when the level is too high. Also the temperature sensor C and D are LOW when the temperature is too low. Design a logic circuit that will detect whenever the level in tank A and B is too high at the same time that the temperature in either tank C and D is too low.

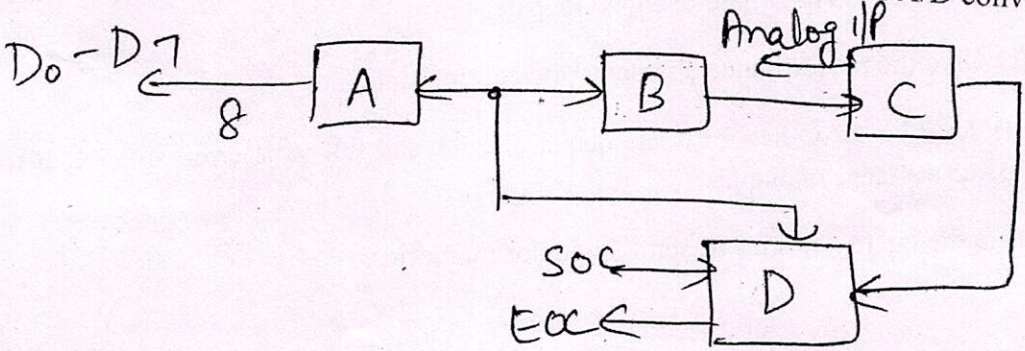
P.T.O.

Q4. Design a counter with T flip flops that goes through the following binary repeated sequence 0,1,3,7,6,4. Show that when binary states 010 and 101 are taken as don't care conditions, counter may not operate properly. Find a way to correct the design.

Part - B

Q5. Explain binary weighted DAC with its circuit diagram and give one example of conversion.

Q6. Consider the below block diagram of a successive approximation A/D converter-



Name correctly the blocks with codes A, B, C, and D. Now, explain each of the named blocks with suitably to justify the working of a successive approximation A/D converter.

Q7. Write brief notes on: FPGA and CPLDS.

x-x-x