Exam.Code:0916
Sub. Code: 6400

2014

B.E. (Computer Science and Engineering)

Fourth Semester

CS-405: Computer Architecture and Organization

Time allowed: 3 Hours **Max. Marks: 50**

NOTE: Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Section.

x-x-x

1. (a) Explain the terms latency and bandwidth. **[5 x 2 = 10]**

(b) Write a short note on Floating point representation.

(c) State the need for introducing L1 and L2 caches separately.

(d) Which parameters influence the choice of page size in virtual memory systems?

(e) Explain dynamic branch prediction algorithm when branch instruction is written at the end of loop.

SECTION – A

2. (a) Explain various addressing modes with the help of examples. [5]

(b) Consider a linked list data structure. Write FIND and DELETE routines that transfer data between a processor register and the linked - list. State your assumptions clearly and explain your solution with the help of an example. [5]

3. (a) Show the control steps needed to implement Brach – to – Subroutine instruction of processors. Draw internal organization of processor as assumed for solving above stated problem. [5]

(b) Write a program to perform sorting of numbers using bubble sort algorithm. State your assumptions clearly and explain your solution with the help of an example. [5]

4. (a) Draw and explain the flowchart for the following: [6]

i) 2's complement addition/subtraction algorithm flowchart with example

ii) 2's complement multiplication algorithm flowchart with example

(b) Compare hardwired and microprogrammed control units. [4]

P.T.O.

SECTION – B

5. (a) Draw and explain synchronous DRAM. Also explain its burst mode with the help of an example. [5]

(b) A block – set – associative cache consists of a total of 64 blocks divided into 4 – block sets. The main memory contains 4096 blocks, each consisting of 128 words.

i) How many bits are there in each of TAG, SET and WORD fields? [3]

ii) What will be the impact of increasing or decreasing size of cache blocks? Explain your answer with example. [2]

6. (a) Assume that in daisy chain bus arbitration arrangement, the processor keeps asserting BG1 as long as *BR* is asserted. When device i is requesting the bus, it becomes the bus master only when it receives a low – to – high transition on its BGi input.

i) Assume that devices are allowed to assert the BR signal at any time. Give a sequence of events to show that the system can enter a deadlock situation, in which one or more devices are requesting the bus, the bus is free, and no device can become the bus master. [2]

ii) Suggest a rule for the devices to observe in order to prevent this deadlock situation from occurring. [2]

(b) Explain distributed bus arbitration with the help of an example. [2]

(c) A computer has one delay slot. The instruction in this slot is always executed, but only on speculative basis. If a branch does not take place, the results of that instruction are discarded. What is speculative execution? Also, suggest a way to implement program loops efficiently on this computer (before and after scenario comparison should be included). [4]

7. (a) A program loop ends with a conditional branch to the beginning of the loop. How would you implement this loop on a pipelined computer that uses delayed branching with one delay slot? Give an example to justify your implementation. [5]

(b) Write a note on Interrupt driven I/O. [5]

x-x-x