Exam.Code:0906 Sub. Code: 6238

2014

B.E. (Computer Science and Engineering) **Second Semester** CS-203: Digital Electronics and Logic Design

Time allowed: 3 Hours

Max. Marks: 50

NOTE: Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Section.

x-x-x

İ	a	Differentiate between multiplexer and demultiplexer.			
	b	What are the applications of 'D' flip-flop?			
	c	List the characteristics of standard TTL and open collector TTL			
	d	Give difference between Synchronous and Asynchronous counters.			
	e	What are the applications of shift registers? (5 X 2 =			
		Section A			
П	a	Design and explain BCD to 7-segment decoder. (5)			
	b	What is carry look-ahead adder? Explain with the help of suitable circuit diagram.			
		(5)			
III	a	Simplify the Boolean expression using K-MAP			
		$Y(A, B,C,D) = \sum m(1,2,3,8,9,10,11,14) + d(7,15) $ (5)			
	b	What are universal gates? Implement XOR and OR gates using minimum number of NAND gates only? (5)			
IV	a	Explain parity generator and checker with circuit diagram. (5)			
	b	Explain conversion of Gray to Binary. Design 3 bit Gray to Binary code converter with the help of suitable circuit diagram. (5)			
		Section B			
V	a	Design Full adder circuit using 4:1 multiplexer (two in number only). (5)			
	b	Design synchronous counter using T flip-flop to count the following sequence 0,5,6,3,7,4,1			

Contd.....P/2

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(2)

	Avoid lockout condition.	(5)		
a	Explain J-K flip flop. Why master slave flip flop is used?	(5)		
b	b What do you mean by counters. Implement 3 bit up-down asynchronous counter			
		(5)		
	Write a short note on:			
a	FPGA and its applications.	(5)		
b	State Reduction and State Assignment.	(5)		
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	b	 a Explain J-K flip flop. Why master slave flip flop is used? b What do you mean by counters. Implement 3 bit up-down asynchronous Write a short note on: a FPGA and its applications. 		