Exam.Code:0929
Sub. Code: 33664

2124

B.E. (Electronics and Communication Engineering)
Fifth Semester
EC-501: VLSI Design

Time allowed: 3 Hours **Max. Marks: 50**

NOTE: Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Section.

x-x-x

1.

a) Define integrated circuits (ICs) and explain their classification. ?

b) What is the significance of Stick diagram in VLSI Design?

c) What is thermal oxidation, and why is it important?

d) Differentiate between Power Dissipation and Power consumption in the ICs.

e) What is the function of nMOS pass transistors in digital circuits?

Section A

2. Describe clocked-CMOS logic and its applications. Discuss the advantages of this design style in dynamic logic circuits.
3. What is Plasma etching? explain the concept with the Sputtering etching Mechanism.
4. Discuss the various steps in sequences to fabricate the N well CMOS (with diagrams)

Section B

5. (a)Explain the structure and operation of a MOSFET. Discuss how the threshold voltage and body bias concepts influence its performance.

   (b)write a short note on the Volage threshold and Body bais concept

6. (a) Consider a CMOS inverter circuit with the following parameters : VDD = 3.3 V, $V_{TO,n}$ 0.6 V, $V_{TO,P} = -0.7$ V, $_{kn} = 200\ \mu A / V^2$, $_{kp} = 80\ \mu A / V^2$ Calculate the noise margins of the circuit. Notice that the CMOS inverter being considered here has $k_R = 2.5$ and $V_{TO,n} V \neq _{TO,P}$ hence it is not a symmetric inverter.)

   (b) write a short note on Metallization in chip fabrication.

7. Define delay time, rise time, and fall time in the context of a CMOS inverter. Discuss the significance of static power dissipation and dynamic power dissipation in CMOS technology.

x-x-x