2124
B.E. (Electrical and Electronics Engineering)
Third Semester
EE-307: Analog and Digital Electronics

Time allowed: 3 Hours   Max. Marks: 50

NOTE: Attempt five questions in all, including Question No. I which is compulsory
and selecting two questions from each Section.

x-x-x

1. (a) Briefly describe the parameters affecting the bias stabilization of a transistor.
   (b) Describe slew-rate of an op-amp.
   (c) Covert the following to other canonical form: $F(x, y, z) = \Sigma(1,3,5,7)$.
   (d) Differentiate edge triggering and level triggering.
   (e) Find the 10's complement of $(935)_{11}$.

   (5×2)

Section-A

2. (a) For the voltage-divider bias configuration shown in figure, determine I_{BQ}, I_{CQ}, V_{CEQ}, V_C, V_E, V_B. (5)
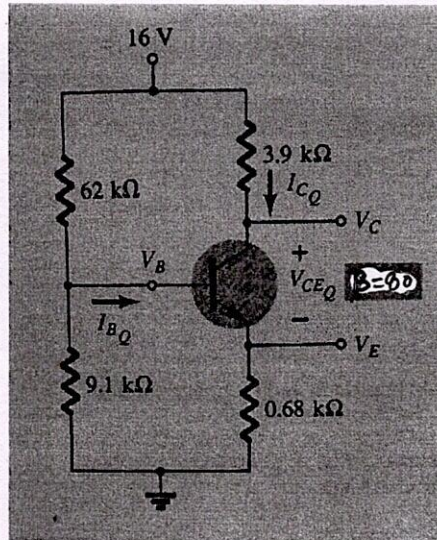
(b) Given $I_E(dc) = 1.2mA$, $\beta = 120$, $r_0 = 40\ k\Omega$, sketch the common-emitter hybrid equivalent model. (5)

3. (a) Calculate the gain, input, and output impedances of a voltage-series feedback amplifier having $A = -300$, $R_i = 1.5\ k\Omega$, $R_0 = 50\ k\Omega$, and $\beta = -1/15$. (5)

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(b) Describe the working of a phase-shift oscillator. What are the conditions for a feedback circuit to be used as an oscillator? (5)

4. (a) Describe the differential and common-mode operation of an op-amp. Calculate the CMRR (in dB) for the circuit with $V_d = 1\ mV$, $V_0 = 120\ mV$, and $V_C = 1\ mV$. Make any required assumptions. (5)

(b) Describe the application of op-amp as a low-pass active filter. (5)

Section-B

5. (a) Simplify the Boolean expression and implement SOP form for (5)

$$F(A,B,C,D) = \sum m(0,3,4,6,7,9,11,13)$$

(b) Implement the function using a 8×1 multiplexer and external gates (5)

$$F(A,B,C,D) = \sum m(1,2,3,7,10,11,12)$$

6. (a) Describe the working of a master-slave flip-flop. How does it avoid race-around condition? (5)

(b) Design a 3-bit synchronous counter going through the states: 1, 2, 6, 7. (5)

7. (a) Describe the working of counter-ramp type analog to digital converter with the help of a block diagram. Determine the resolution of a 10-bit A/D converter having a full scale analog input voltage of 5 V. (5)

(b) Describe the working of a sample and hold switch. (5)

x-x-x