Exam.Code:0969
Sub. Code: 34528

2124

M.E. (Electronics and Communication Engineering)

First Semester

ECE-1104: Digital System Design

(For UIET Only)

Time allowed: 3 Hours | Max. Marks: 50

***NOTE**: Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Unit.*

x-x-x

I. Attempt the following:-

a) Why commercial ECL families are not as popular as CMOS and TTL?

b) Define speed-power product. What is its significance?

c) Differentiate between combinational and sequential circuits.

d) What are the types of memory?

e) What is Testability? (5x2)

UNIT - I

II. Draw the block diagram of PAL and explain the design aspects used in PAL. (10)

III. Define a combinational circuit. Draw the block diagram, explain the steps involved in designing the combinational circuit. (10)

IV. Explain the concepts of A/D conversions along with related errors. (10)

UNIT - II

V. Write short notes on:-

a) Fault diagnosis

b) Fault detection

c) Test generation in digital circuits (10)

VI. Design positive edge triggered JK flip-flop and explain its functional and timing behaviour. Also write a VHDL program. (10)

VII. Explain the architecture of Built in self-test and discuss its operation briefly. (10)

x-x-x