Exam.Code:0916
Sub. Code: 6400

2053

B.E. (Computer Science and Engineering)

Fourth Semester

CS-405: Computer Architecture and Organization

Time allowed: 3 Hours Max. Marks: 50

NOTE: *Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Section.*

x-x-x

Q 1. (a) Explain the protocols used for handling a write miss in cache memory. **[5 x 2 = 10]**

(b) How will you check overflow in case of 2's complement representation?

(c) State the advantage of indirect addressing mode over direct addressing mode with the help of an example.

(d) Compare RISC and CISC machines based on performance parameters.

(e) Explain data hazard in pipelining and also state a possible solution for the same.

SECTION – A

Q 2. (a) Differentiate between synchronous and asynchronous bus. [3]

(b) Write a note on assembler directives. [3]

(c) Draw and explain multiple bus processor organization. [4]

Q 3. (a) Explain the microprogrammed control unit. [4]

(b) Show how a 9-bit microoperation field in a microinstruction can be divided into subfields to specify 46 microoperations. How many microoperations can be specified in one microinstruction. [3]

(c) Write a program to perform in-place sorting of "n" numbers. State your assumptions clearly and explain your solution with the help of an example. [3]

Q 4 (a) Write a note on floating point representation. [3]

(b) Show the contents of registers E, A, Q and SC during process of division of 10100011 by 1011. Also draw the flowchart and perform step–by–step run to achieve your values. [7]

SECTION – B

Q 5. (a) A block-set-associative cache memory consists of 128 blocks divided into four block sets. The main memory consists of 16,384 blocks and each block contains 256 eight bit words. How many bits are needed to represent the TAG, SET and WORD fields? [4]

(b) A computer system has main memory consisting of 1M 16-bit words. It also has a 4K – word cache organized in the block – set – associative manner, with 4 blocks per set and 64 words per block.

i) Calculate the number of bits in each of the TAG, SET, and WORD fields of the main memory address format. [3]

P.T.O.

ii) Assume cache is initially empty. Suppose that processor fetches 4352 words from location 0, 1 , . . . , 4351, in that order. It then repeats this fetch sequence nine more times. If the cache is 10 times faster than the main memory, estimate the improvement factor resulting from the use of cache. Assume that LRU replacement algorithm is used for block replacement. [3]

Q 6. (a) Assume two DMA devices are attached to processor using daisy chain bus arbitration arrangement. Draw and explain sequence of various control signals during transfer of bus mastership for the two DMA devices. [4]

(b) A computer has one delay slot. The instruction in this slot is always executed, but only on speculative basis. If a branch does not take place, the results of that instruction are discarded. What is speculative execution? Also, suggest a way to implement program loops efficiently on this computer (before and after scenario comparison should be included). [6]

Q 7. (a) Explain how dynamic branch prediction works to reduce the probability of making wrong decision. Give appropriate examples to support your claim. [6]

(b) Write a note on Interrupt – driven I/O. [4]

x-x-x