Exam.Code:0976 Sub. Code: 7115

2063

M. Tech. (Microelectronics) **Second Semester**

MIC-204: Advanced Memory Technology and Design

Time allowed: 3 Hours Max. Marks: 50

NOTE: Attempt <u>five</u> questions in all, including Question No. I which is compulsory and selecting two questions from each Part.

·1.	a) Discuss working principle of 1-T memory cell?b) Why CMOS technology is most suitable for memory circuits?	(2)
	c) What do you understand by scaling law in memoires?	(2)
	d) Briefly discuss significance of S/N ratio in memory design?	(2)
	e) What is the function of the word line in memory circuits?	(2)
	PART-A	
2.	a) Explain working of any NMOS dynamic logic circuit.	(5)
	b) Enumerate read and writing operation to a flash memory cell. What are the a	dvantages of
	using flash memory cells in a computer system?	. (5)
3.	a) What are non-volatile memories? Discuss standard specification of various no	on-volatile
	memories.	(5)
	b) How does the scaling of feature size affect the switching speed and capacitan	ce of MOS
	transistors?	(5)
4.	What are voltage converters? Describe (Up OR Down) architecture of Voltage Converters in	
	details.	(10)
	PART-B	
5.	a) What is data line noise in DRAM circuits? How does data line noise impact the and performance of DRAM circuits?	
	b) List various techniques used to reduce data line noise in DRAM circuits? D	(5)
	technique in detail.	escribe any one (5)
6.	a) What is fault tolerance in memory organizations, and why is it important?b) List different redundancy techniques used to realize fault tolerance in memory.	(5)
	Discuss any one technique in detail.	y organizations.
7.	Write Short note on following: -	(2.5 x 4=10)
	a) Multi-divided data line	(=10 11 1 10)
	b) On-chip testing circuits	
	c) Refresh relevant circuits	
	d) Address multiplexing	