Exam.Code:0970
Sub. Code: 7054

2063

M.E. (Electronics and Communication Engineering)

Second Semester

ECE-1205: VLSI Design

Time allowed: 3 Hours Max. Marks: 50

NOTE: *Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Unit.*

x-x-x

I. Explain the following:-

a) Need of Sequencing method

b) Max-delay Constraints

c) Logic synthesis

d) Silicon Wafer

e) Delay Constraint (5x2)

UNIT - I

II. (a) Explain static CMOS and Pass transistor circuit.

(b) Explain time borrowing and clock skew with the help of suitable diagrams. (2x5)

III. (a) Explain the various steps involved in VLSI design flow.

(b) Explain logic design for data path subsystems. (2x5)

IV. Explain the following with the help of diagrams:-

(a) Twin Tub

(b) Silicon on Insulator processing (2x5)

UNIT - II

V. Explain fully custom design with the help of diagrams and various CAD tools available in VLSI design process. (10)

VI. Explain high level and logic synthesis. (10)

VII. Explain the following with the help of diagrams:-

(a) Hierarchy of Simulation Tools

(b) Spice simulation tool (2x5)

x-x-x