Exam.Code:0906
Sub. Code: 6258

2063

B.E. (Electronics and Communication Engineering)

Second Semester

EC-203: Digital Design

Time allowed: 3 Hours **Max. Marks: 50**

NOTE: Attempt five questions in all, including Question No. 1. (Section-A) which is compulsory and selecting two questions each from Section B-C.

x-x-x

	Section A	
1	i. What is universal gate? Realize AND gate using universal gates. ii. Differentiate canonical and standard form of a Boolean expression. iii. What is a lockout condition in a counter and how it is avoided? iv. Write down specifications of D/A converters. v. Define noise margin and noise immunity of a logic family.	10
	Section B	
2	a) Obtain the set of prime implicants for $\sum m(0,1,6,7,8,9,13,14,15)$ using Q-M method. b) What is race around condition in a flip-flop? How it can be avoided?	5 5
3	a) Implement a full adder with two 4x1 multiplexers. b) With suitable diagram explain working of a BCD adder.	5 5
4	a) Convert D to T and S-R to J-K flip-flops. b) List the PLA programming table for BCD to excess-3 code converter.	5 5
	Section C	
5	a) Design a 3-bit synchronous counter to count sequence 0,1,4,6,7 and repeat using J-K flip-flop. b) What is universal shift register? Draw and explain a 4-bit universal shift register controlled by 4x1 multiplexers.	5 5
6	a) What are the drawbacks of weighted-resistor D/A converter? How these drawbacks can be overcome using modified weighted-resistor D/A converter? b) Compare TTL, ECL and CMOS logic families based on their characteristics.	5 5
7	a) Explain construction and working of totem pole TTL. Why it is advantageous over open collector TTL. b) Differentiate a ring counter and twisted ring counter. Explain working of 4-bit Johnson's counter.	5 5

x-x-x