Exam.Code:0906
Sub. Code: 6258

2023

B.E. (Electronic and Communication Engineering), Second Semester

EC-203: Digital Design

Time allowed: 3 Hours **Max. Marks: 50**

NOTE: Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Section. Use of scientific calculator is allowed.

x-x-x

I. (a) What are counters? Give difference between asynchronous and synchronous counters. (2)

(b) What type of codes are used in K-map designing and why? (2)

(c) Differentiate between encoder and decoder on the basis of communication system. (2)

(d) Which is the fastest logic family and why? (2)

(e) Explain the two major drawbacks of binary weighted resistor D/A converter. (2)

Section-A

II. (a) Solve the following using K-map and implement the circuit using NAND gates only

$$F = \sum m(0,2,3,8,11,12) + d(1,9,14)$$ (5)

(b) What is the concept of flip-flop in an electronic circuit? Explain JK flip-flop. (5)

III. (a) What are essential prime implicants? How are they different from simple prime implicant groups? (5)

(b) What are universal gates? Design half adder circuit using minimum number of NOR gates. (5)

IV. (a) Explain multiplexer and implement the following function using single 4:1 multiplexer

$$f(A,B,C) = \sum m(0,2,3,7)$$ (5)

(b) What is a digital comparator? Explain single bit digital comparator. (5)

Section-B

V. (a) Explain binary ladder type D/A converter. (5)

(b) Explain flash type A/D converter with the help of an example. (5)

VI. (a) Design and explain the circuit of ECL OR/NOR gate. (5)

(b) Give comparison of CMOS, ECL and TTL logic families on the basis of their performance parameters. (5)

VII. (a) Design a synchronous counter using JK flip-flops to count the following sequence

0,2,5,6,7

Avoid lockout condition. (5)

(b) Explain four bit PISO shift register with the help of suitable diagram. (5)

x-x-x