Exam. Code: 0906
Sub. Code: 6238

2023

B. Engg. (Computer Science and Engineering)-2nd Semester

CS-203: Digital Electronics and Logic Design

Time allowed: 3 Hours **Max. Marks: 50**

NOTE: ***Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Section.***

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1. (a) Find the 10's complement of $(832)_{11}$.

   (b) Covert the following to other canonical form: $F(x, y, z) = \sum(1,3,5,7)$.

   (c) What is race around condition? How can it be avoided?

   (d) Describe the meaning and importance of *fan out* in a logic family.

   (e) Design a 2-bit magnitude comparator.

   (5×2=10)

Section-A

2. (a) Describe ECL OR/NOR gate with the help of circuit diagram. Compare ECL with other logic families. (5)

   (b) Simplify the following Boolean expression using Quine-Mcclusky method: (5)

$$F(A, B, C, D, E) = \sum m(1, 2, 5, 6, 8, 10, 11, 16, 18,19,23,27,28)$$

3. (a) Describe CMOS NAND gate using circuit diagram. What is the reason behind low power consumption of this family? (5)

   (b) Design a parity generator and checker for a 4-bit binary number. (5)

4. (a) Simplify the following Boolean expression: (5)

$$F(A, B, C, D) = \prod M(0,3,4,5,6,7,11,15) + d(1,9,10,13)$$

   (b) Design a carry look-ahead adder for 4-bit binary numbers. (5)

Section-B

5. (a) Implement the following function using a 8×1 multiplexer: (5)

$$F(A, B, C, D) = \sum m(0,3, 5, 7, 8, 12, 13)$$

   (b) Show how two IC 7483 can be used for adding two 4-bit numbers. (5)

6. (a) Design a self-correcting synchronous counter going through states 0,1,4,5. All unused states should lead to state '000'. (5)

   (b) Design a universal shift register using IC 74194 having features of shift-left, shift-right, hold, and parallel input features. (5)

7. (a) Design a Mod-6 asynchronous up-down counter. (5)

   (b) Describe FPGA and its applications. (5)

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