2023

M. Tech. (Micro-Electronics) First Semester MIC-109: Hardware Description Languages

Time allowed: 3 Hours Max. Marks: 50

NOTE: Attempt <u>five</u> questions in all, including Question No. I which is compulsory and selecting two questions from each Unit.

Y-Y-Y

- I. Attempt the following:
 - a) Briefly discuss top-down methodology using suitable example.
 - b) List advantages of HDLs over sequential programming languages.
 - c) Discuss precedence of operators in VHDL.
 - d) Write VHDL code for half-adder.
 - e) Why Verilog is preferred over VHDL nowadays?

(5x2)

UNIT-I

- II. a) Discuss significant features of VHDL.
 - b) Design 4x1 Multiplexer using 2x1 Multiplexer and write VHDL code.

ock Write test

(2x5)

- III. a) Write VHDL code for D flip-flop with negative edge triggered clock. Write test bench to verify its functionality.
 - b) What are different types of architectures available in VHDL? Give Suitable examples. (2x5)
- IV. a) Discuss importance of process statement in VHDL.
 - b) Design and write code of 3x8 decoder using when else statement. (4,6)

UNIT - II

- V. a) Design and write Verilog HDL code for 4-bit down-counter.
 - b) List key difference between VHDL and Verilog HDL.

(2x5)

- VI. a) Describe Predefined attributes in VHDL using an example.
 - b) Design full adder using structural modelling style.

(2x5)

P.T.O.

(2)

VII. Write short note on the following:-

- a) Sequential Wait Statement
- b) Advanced Arithmetic Operators
- c) Modules (in Verilog)
- d) Configurations

 $(4x2\frac{1}{2})$

x-x-x