2023
M. Tech. (Micro-Electronics)
First Semester
MIC-103: MOS Integrated Circuit Modeling

Time allowed: 3 Hours   Max. Marks: 50

NOTE: *Attempt* <u>*five*</u> *questions in all, including Question No. 1 which is compulsory and selecting two questions from each Unit.*

x-x-x

I.   Attempt the following:-

   (a) Compare CMOS and bipolar technologies.

   (b) Why is NMOS technology more preferred than PMOS technology?

   (c) Define feature size and state the objectives of layout design rules.

   (d) What is body effect?

   (e) What is the purpose of a latch circuit? Draw one latch and explain.   (5x2)

UNIT - I

II.   a) Explain the basic structure, operation and drain current characteristics of a depletion type MOSFET.

   b) Consider the following p-channel MOSFET process: Substrate doping $ND = 1015$ cm-3, polysilicon gate doping density $ND = 1020$ cm-3, gate oxide thickness $tx = 650$ A, and oxide-interface charge density $Nox = 2 \times 1010$ cm-2. Use $Esi = 11.7 EO$ and $Eox = 397 EO$ for the dielectric coefficients of silicon and silicon-dioxide, respectively, (i) Calculate the threshold voltage V, for $VSB = 0$. (ii) Determine the type and the amount of channel ion implantation which are necessary to achieve a threshold voltage of $V=-2V$.   (10)

III. a) Discuss the Noise Margins for the CMOS Digital Integrated circuits with Help of logic families.

   b) Explain CMOS inverter with its equivalent circuit.   (10)

IV.   a) Explain the different type of CMOS inverter switching.

   b) Explain in delay about RC delay estimation with suitable examples.   (10)

P.T.O.

UNIT - II

V. Sketch the logic gate symbolic representation of an JK Flip- flop using NAND gates. Give the truth table and describe the operation. Also sketch a CMOS circuit implementation. (10)

VI. Write a short note on:-

(a) CMOS Transmission gate

(b) BICMOS Logic (10)

VII. Draw a full adder circuit with CMOS logic and explain the functionality with help of Truth table. (10)

x-x-x