Exam.Code:0969 Sub. Code: 7046

2023

M.E. (Electronics and Communication Engineering)

First Semester ECE-1104: Digital System Design

(For UIET)

Time allowed: 3 Hours

Max. Marks: 50

**NOTE**: Attempt <u>five</u> questions in all, including Question No. I which is compulsory and selecting two questions from each Unit.

x-x-x

- I. Attempt the following:
  - a) Logic representation of system
  - b) What is sampling Error?
  - c) Explain state diagram
  - d) Explain Cycles and races.
  - e) What is the difference between CLBs and Function blocks? (5x2)

## UNIT - I

- II. a) Explain XC 4000 and its various blocks with the help of diagrams.
  - b) Explain analog and digital conversion related errors.

(2x5)

- III. a) Write VHDL source code for a priority Encoder.
  - b) Explain Generic Array Logic. How GAL differs from PAL?

(2x5)

IV. A combinational circuit is defined by the functions:

$$F_1$$
 (A,B,C) =  $\Sigma$ (3,5,6,7)

$$F_2(A,B,C) = \Sigma(0,2,4,7)$$

Implement the circuit with a PLA having three inputs, four product terms, and two outputs. (10)

## UNIT - II

- V. a) Define state reduction. What are the rules for state reduction?
  - b) Explain FSMs. With the help of diagram, explain all the categories of FSM. (2x5)

P.T.O.

VI. a) Design a modulo 10 Gray Code decade counter which can be cascaded with other identical counters to form a modulo n pure synchronous counter. This counter is to be designed to function identical to the 74160 series of counters.

$$(Sequence: \rightarrow 0 \rightarrow 1 \rightarrow 3 \rightarrow 2 \rightarrow 6 \rightarrow 14 \rightarrow 10 \rightarrow 11 \rightarrow 9 \rightarrow 8)$$

- b) Explain state reduction. Explain the two basic rules for making state assignment. (6,4)
- VII. a) Design a special circuit that will produce an output pulse if a sampled data input is tested three times and found to be at a relatively high voltage level an odd number of times, and will then return to an initial condition and start the testing process over again.
  - b) Explain internal scan test methodology and BIST. (2x5)