Exam.Code:0999
Sub. Code: 7295

2023

M.E. (Computer Science and Engineering)

First Semester

CS-8109: Advance Computer Architecture

(For UIET)

Time allowed: 3 Hours **Max. Marks: 50**

NOTE: Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Section.

x-x-x

1 Explain in brief

a) Blocking vs. Non-blocking networks.
b) Spatial vs. Temporal parallelism.
c) What is CPI and its formula?
d) Control flow vs. data flow.
e) Compare Amdahl's law and Gustafson's law with appropriate diagram .

(02x05)

Section A

2 a) Consider the interleaved execution of the four programs as follows on each of the three machines. Each program is executed in a particular mode with the measured MIPS rating.

Programs	Execution Time (in seconds)		
	Computer A	Computer B	Computer C
Program 1	1	10	20
Program 2	1000	100	20
Program 3	500	1000	50
Program 4	100	800	100

i) Determine the arithmetic mean execution time per instruction for each machine executing the combined workload, assuming equal weights for the four programs.
ii) Determine the harmonic mean MIPS rate of each machine.
iii) Rank the machines based on the harmonic mean performance.

b) What are semaphores and their applications in parallel computing? Compare Binary and Counting semaphores.

(06+04)

3 a) What are VLIW processors? Discuss the various problems associated with the VLIW processor and measures for their mitigation.
b) Explain the Snoopy Bus Protocol with labeled diagrams.

(05+05)

4 Explain the following terms associated with cache design:

a) Write-through vs. write-back caches.
b) Private caches vs. shared caches.
c) Cache flushing policies.
d) Cacheable vs. non-cacheable data.
e) Physical address cache vs. virtual address cache.

(02x05)

P.T.O.

Section B

5 a) Draw and explain block diagram of Backplane Bus System. Also, describe bus arbitration and control.

b) Draw and explain the CM-2 architecture. Explain in detail that how the nodes are processed in CM-2?

(05+05)

6 a) What are inclusion property and memory coherence requirements? Distinguish between write through and write back policies.

b) Write a short note on vectorization and parallelization methods to improve the performance of programs. Compare it with scalar optimization methods.

(04+06)

7 a) Explain various cache coherence and synchronization mechanisms.

b) Analyze the data dependences among the following statements in a given program:

S1: Load R1, 1024 /R1 ← 1024/
S2: Load R2, M (10) /R2 ← Memory (10)/
S3: Add R1, R2 /R1 ← (R1) + (R2)/
S4: Store M (1024), R1 /Memory (1024) ← (R1)/
S5: Store M ((R2)), 1024 /Memory (64) ← 1024/

Where (Ri) means the content of register Ri and Memory (10) contains 64 initially.

i) Draw a dependence graph to show all the dependences

ii) Are there any resource dependences if only one copy of each functional unit is available in the CPU?

(04+06)

x-x-x