Exam.Code:0969 Sub. Code: 7046

2123

M.E. (Electronics and Communication Engineering) First Semester ECE-1104: Digital System Design

(For UIET Only)

Time allowed: 3 Hours

Max. Marks: 50

NOTE: Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Unit.

x-x-x

- Attempt the following:-I.
 - Design Constraints. a)
 - Analog and digital conversion related errors b)
 - Explain state diagram c)
 - Need of modeling & simulation d)
 - Difference between CLBs and Function blocks? e)

(5x2)

UNIT - I

- a) Explain XC 9500 and its various blocks with the help of diagrams. II.
 - b) Explain logic representation of a system.

(2x5)

- a) Write VHDL source code for a priority Encoder. III.
 - b) Explain Generic Array Logic. How GAL differs from PAL?

(2x5)

A combinational circuit is defined by the functions: IV.

$$F_1(A,B,C) = \Sigma(3,5,6,7)$$

$$F_2(A, B, C) = \Sigma(0, 2, 4, 7)$$

Implement the circuit with a PLA having three inputs, four product terms, and two (10)outputs.

UNIT-II

- a) Define state reduction. What are the rules for state reduction? V.
 - b) Explain FSMs. With the help of diagram, explain all the categories of FSM. (2x5)
- a) Design a modulo 10 Gray Code decade counter which can be cascaded with other VI. identical counters to form a modulo n pure synchronous counter. This counter is to be designed to function identical to the 74160 series of counters.

$$(Sequence: \xrightarrow{0 \to 1 \to 3 \to 2 \to 6 \to 14 \to 10 \to 11 \to 9 \to 8 \xrightarrow{})$$

Contd.....P/2

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(2)

- b) Explain state reduction. Explain the two basic rules for making state assignment. (6,4)
- VII. a) Design a special circuit that will produce an output pulse if a sampled data input is tested three times and found to be at a relatively high voltage level an odd number of times, and will then return to an initial condition and start the testing process over again.
 - b) Explain the internal scan test methodology and BIST.

(2x5)