Exam.Code:0977
Sub. Code: 7119

2123

M. Tech. (Micro-Electronics)

Third Semester

MIC-301: Low Power Digital CMOS Design

Time allowed: 3 Hours **Max. Marks: 50**

NOTE: Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Part.

x-x-x

1. Answer the following:-

a. Discuss two limits of hierarchy for low power design.
b. What is the source of power consumption in a CMOS SRAM?
c. Derive the expression for the dynamic power dissipation in a CMOS inverter.
d. Discuss three short channel effects in a MOSFET.
e. Differentiate between average power and maximum power in a digital circuit. (5x2=10)

PART A

2 a. What is an advantage of saving power in digital circuits? What are the applications of low power systems?
b. Give a historical review of the developments in low power design.
c. What are the requirements for a MOSFET model at low power design? Give salient features of any model used for low power design. (2,3,5)

3 What are the methodologies to minimize the power dissipation and propagation delay in digital inverters? Compare these methodologies also. (10)

4 What are the obstacles in minimizing power reduction in digital circuits? How power is estimated in digital circuits? (10)

PART B

5 What is the source of power dissipation in digital buses? How power can be reduced in them? Explain by taking a suitable technique. Hence compare the power dissipation in buses with a CMOS inverter. (10)

6 a. Explain the sources of power dissipation in 6T CMOS SRAM? How the power can be saved?
b. Compare the power dissipation in 6T SRAM and 1T DRAM. How the power can be saved in 1T DRAM. (5,5)

7 Explain how an address decoder, level shifter and a clock of a six transistor SRAM operate at low power? What are the low power design techniques for such circuits? (10)

x-x-x