Exam.Code:0975
Sub. Code: 7079

2123

M. Tech. (Micro-Electronics)

First Semester

MIC-109: Hardware Description Languages

Time allowed: 3 Hours

Max. Marks: 50

NOTE: *Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Unit.*

x-x-x

I. Attempt the following:-

a) What is binding?

b) How Rise, Fall and turn-off delays are specified in Verilog?

c) With syntax describe the continuous assignment statement.

d) What are the primitive gates supported by Verilog HDL?

e) Compare between simulation and synthesis. (5x2)

UNIT - I

II. With syntax explain conditional, branching and loop statements available in VHDL behavioural description. (10)

III. Apply the Bottom-up design methodology to demonstrate the design of 4-bit ripple carry adder. (10)

IV. List and explain the advantages and shortcomings of using VHDL? (10)

UNIT - II

V. With neat sketch explain the digital system design approach using VHDL. (10)

VI. Write Verilog code for signal assignment statement "y=3x" with x as of size bits. Also show the mapping of this signal assignment to gate level. HDL program of 4-bit synchronous up counter. (10)

VII. Consider an example of one-bit full adder, explain the structural specification of hardware and give its structural description using VHDL. (10)

x-x-x