Exam.Code:0975
Sub. Code: 7106

2123

M. Tech. (Micro-Electronics)

First Semester

MIC-103: MOS Integrated Circuits Modelling

Time allowed: 3 Hours Max. Marks: 50

NOTE: Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Unit.

x-x-x

I. Answer the following:-

(a) Define FPGA and explain its significance?

(b) Discuss the method of conversion from binary to grey code.

(c) How Sum of the product minimizing technique work?

(d) Depict the internal structure of synchronous SRAM. (10)

UNIT - I

II. Discuss the VI characteristics of a MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) and its significance in circuit design. (10)

III. Create a schematic for a static CMOS VLSI gate implementing the Boolean function f = (A+B) . (C+D). Clearly depict the pull-up and pull-down networks, and connections to power and ground, and ensure clarity in representing the output f of the logic gate. (10)

IV. Devise a 4-bit ripple-down counter using only 4 flip-flops and no additional components. (10)

UNIT - II

V. Provide the symbolic representation of a JK Flip-Flop using NAND gates. Include the truth table, describe its operation, and additionally, illustrate a CMOS circuit implementation. (10)

P.T.O.

VI. a) Discuss the functionality of a Barrel Shift Register.

b) Explain the concept of Clocking Techniques and their applications. (10)

VII. Write a short note on:-

a) Transmission gate

b) BiCMOS Logics. (10)

x-x-x