Exam.Code:0999
Sub. Code: 7295

2123

M.E. (Computer Science and Engineering)

First Semester

Elective - II

CS-8109: Advanced Computer Architecture

(For UIET)

Time allowed: 3 Hours Max. Marks: 50

NOTE: Attempt five questions in all, including Question No. 1 which is compulsory and selecting two questions from each Section.

x-x-x

Q1 Explain in brief

i) Spatial vs. Temporal parallelism
ii) What is CPI, its importance in parallelism and its formula?
iii) Comment on the advantages and disadvantages in control complexity, potential for parallelism and cost-effectiveness of control and data flow computer models
iv) Difference between semaphores and monitors
v) Compare Amdahl's law and Gustafson's law with appropriate diagram (2x5)

Section A

Q2 a) Consider the execution of an object code with $2x10^6$ instructions on a 400MHz processor.The program consists of four major types of instructions. The instruction mix and the number of cycles (CPI) needed for each instruction type are given below based on the result of a program trace experiment:

Instruction type	CPI	Instruction mix
Arithmetic and logic	1	50%
Load/store with cache hit	2	18%
Branch	3	12%
Memory reference with cache miss	6	10%
Data transfer	4	10%

(i) Calculate the average CPI when the program is executed on a uniprocessor with the above trace results.
(ii) Calculate the corresponding MIPS rate based on the CPI obtained in part (i). (6)
b) Compare architectural characteristic CISC and RISC supercomputers? Explain how to save the design space in RISC computers. (4)

Q-3 a) What are VLIW processors? Discuss the various problems associated with the VLIW processor and measures for their mitigation.
b) Explain the Snoopy Bus Protocol with labeled diagrams. (5x2)

Q-4 Explain the following terms:

i) Bernstein Conditions for parallelism
ii) Cache flushing policies
iii) Compare Omega and Baseline network
iv) Draw any SPARC architecture
v) Physical address cache vs. virtual address cache (5x2)

Section B

Q-5 a) Draw and explain the architecture of IBM RISC system/6000 superscalar processor.
b) How performance of parallel processors is measured? With relevant graphs, discuss the performance of distributed shared memory multiprocessors (5x2)

Q-6 a) What are inclusion property and memory coherence requirements? Distinguish between write through and write back policies used for cache coherence.
b) Explain the applicability and the restrictions involved in using Amdahl's law, Gustafson's law and Sun and Ni's law to estimate the speedup performance of an n-processor system compared with that of a single-processor system. Ignore all communication overheads. (5x2)

Q-7 a) Explain various cache coherence and synchronization mechanisms. (4)
b) Analyze the data dependences among the following statements in a given program:

S1: Load R1, 1024 */R1 ← 1024/*
S2: Load R2, M (10) */R2 ← Memory (10)/*
S3: Add R1, R2 */R1 ← (R1) + (R2)/*
S4: Store M (1024), R1 */Memory (1024) ← (R1)/*
S5: Store M ((R2)), 1024 */Memory (64) ← 1024/*

Where (R_i) means the content of register R1 and Memory (10) contains 64 initially.

i) Draw a dependence graph to show all the dependences
ii) Are there any resource dependences if only one copy of each functional unit is available in the CPU? (6)

x-x-x