Exam.Code:0976
Sub. Code: 7432

2072

M. Tech. (Microelectronics)

Second Semester

MIC-209: Digital Integrated Circuits Design

Time allowed: 3 Hours Max. Marks: 50

NOTE: *Attempt five questions in all, including Question No. 1 (Section-A) which is compulsory and selecting two questions each from Section B-C.*

x-x-x

SECTION-A

1. a) Explain the following terms.
   i. Logic Levels ii. Noise margin

   b) What is the difference between transmission time and propagation delay?

   c) Compare PLA and PAL.

   d) What are the different types of tri state buffers ?

   e) Write the difference between latches and flip flops. (5*2=10)

SECTION B

2) a). Describe the rules for state assignment. Give an example? (5)

   b). What is clock skew? How it is calculated? (5)

3) a). Explain how to estimate propagation delay? (5)

   b). Find the minimized PLA of the following output Boolean function by a PLA minimizer :

   f1 = (2,4,5,6,7,10,14,15): f2 = (4,5,7,11,15) (5)

4) Explain the delay in combinational logic network and how combinational delay can be reduced. Give two examples of metastability that occur in everyday life. (10)

SECTION C

5) Design a data unit and a control unit state machine for multiplying 8 bit 2's complement number. (10)

6) Design a barrel shifter using 16 data inputs, 16 data outputs and 4 control inputs. (10)

7) a) Explain how the extracting a data path and controller from the ASM chart. (5)

   b) Explain how would you translate a register transfer structure into a legal two phase latched sequential machine give an example (5)

x-x-x