Exam.Code:0970
Sub. Code: 7347

2072

M.E. (Electronics and Communication Engineering)

Second Semester

ECE-1205: VLSI Design

Time allowed: 3 Hours

Max. Marks: 50

NOTE: *Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Part.*

x-x-x

1) Attempt the following:-

a. Differentiate between the capacitive behavior of a MOSFET in depletion and inversion regions.
b. Explain why the ON current saturates in a MOSFET.
c. Differentiate between an active resistor and a passive resistor.
d. How is clock line distributed in physical layout?
e. Give salient features of a CAD tool. (5x2=10)

PART A

2) a. Differentiate between the weak inversion and moderate inversion regions of a MOSFET.
b. Draw and explain the transfer characteristics of a MOSFET.
c. Explain the term "body effect" in a MOS transistor. (4,3,3)

3) a. Compare the working of a depletion load MOSFET inverter and a CMOS inverter.
b. Compare the NMOS and PMOS pass transistors.
c. Differentiate between static power and dynamic power dissipation in a CMOS inverter. (4,3,3)

4) Write notes on:-

a. CMOS NAND logic gate
b. Delay minimization in CMOS circuits (5,5)

PART B

5) a. Differentiate between floor planning and placement techniques in a physical layout design.
b. What is compaction in VLSI layout? Explain the different types of compaction techniques.
c. What is a CAD tool? Give two salient features of a CAD tool. (4,4,2)

6) a. Differentiate between a semicustom and full custom design for VLSI circuits.
b. Explain how a layout can be synthesized?
c. Compare global and local routing techniques. (4,3,3)

7) Write notes on:
a. FPGA based design
b. Lambda rules

(5,5)

x-x-x