Exam.Code:0906
Sub. Code: 6682

2072

B.E. (Electronics and Communication Engineering)

Second Semester

EC-203: Digital Design

Time allowed: 3 Hours

Max. Marks: 50

NOTE: *Attempt five questions in all, including Question No 1 which is compulsory and selecting two questions from each Section. Use of scientific calculator is allowed.*

x-x-x

I. **(a)** Solve the following conversion and find the value of 'x' for:

$$(365)_x = (194)_{10}$$ **(2)**

(b) What type of codes are used in K-map designing and why? **(2)**

(c) What are unsaturated logic families? Give its significance. **(2)**

(d) How many flip-flops are required to design Decade counter? Give its applications. **(2)**

(e) Explain the role of SIPO shift register. **(2)**

Section-A

II. **(a)** Solve the following using K-map and implement the circuit using NAND gates only

$$F(A,B,C,D) = \sum m(3,4,5,7,9,13,14,15)$$ **(5)**

(b) What is race around condition? How it can be eliminated? **(5)**

III. **(a)** What is comparator? Design two-bit magnitude comparator. **(5)**

(b) Convert JK flip-flop into D flip-flop. **(5)**

IV. **(a)** State and proof DeMorgan's Theorems. Explain with the help of example how it is useful for designing using universal gates? **(5)**

(b) What is a code converter? Explain binary to gray code converter. **(5)**

Section-B

V. **(a)** Explain the drawbacks of binary weighted resistance type D/A converter. How these drawbacks can be removed? **(5)**

(b) Explain successive approximation type A/D converter with the help of an example. **(5)**

VI. **(a)** Give comparison of TTL, ECL and MOS on the basis of characteristics such as fan-in, fan-out, power dissipation, propagation delay and noise margin. **(5)**

(b) Design the circuit of TTL NAND gate and explain its working. **(5)**

VII. **(a)** Design a synchronous counter using T flip-flop to count the following sequence

0,5,6,3,7,4,1

Avoid lockout condition. **(5)**

(b) Explain universal shift register with the help of suitable diagram. **(5)**

x-x-x