15/12/22(M)

Exam.Code:0929
Sub. Code: 6593

2122

B.E. (Electronics and Communication Engineering)
Fifth Semester
EC-501: VLSI Design

Time allowed: 3 Hours Max. Marks: 50

NOTE: *Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Unit.*

x-x-x

I. Attempt the following:-

a) Discuss the Classification of the Integrated circuits.

b) What is Layout Design in VLSI design flow?

c) Write a short note on short channel effects.

d) Differentiate between Power Dissipation and Power consumption in the ICs.

e) Discuss the basic principle of the MOS Pass Transistor. (5x2)

UNIT - I

II. a) Different between wet and dry etching used in IC fabrication

b) How Crystal Growth occurs for the preparation of the wafer (CZ method). (2x5)

III. a) What is CVD? Explain the various technologies used for the deposition of material in IC manufacturing.

b) Describe the Mechanism of Epitaxial growth. (2x5)

IV. Discuss the various steps in sequences to fabricate the N well CMOS (with diagrams). (10)

UNIT - II

V. a) Explain pass transistor logic with illustrative examples. Explain how transmission Gate logic is preferable over pass transistor logic.

b) Draw a full adder circuit with CMOS logic and explain the functionality with help of Truth table. (2x5)

P.T.O.

VI. a) Differentiate between Static Power Dissipation and dynamic Power consumption in the CMOS.

b) Consider a CMOS inverter circuit with the following parameters:

VDD = 3.3 V, $V_{T0,n}$=0.6 V, $V_{TO.P}$ = -0.7 V, $_{kn}$ = 200 μA/V^2, $_{kp}$ = 80 μA/ V^2 Calculate the noise margins of the circuit. Notice that the CMOS inverter being considered here has k_R = 2.5 and $V_{T0,n}$ V≠ $_{TO,P}$ hence it is not a symmetric inverter.

(2x5)

VII. Write a short note on:-

a) Noise Margin of CMOS Inverter

b) Enhancement type MOSFET (2x5)

x-x-x