Exam. Code: 0977
Sub. Code: 7120

2122

M. Tech. (Microelectronics) Third Semester

MIC-302: Microelectronic Packaging and Testing

Time allowed: 3 Hours Max. Marks: 50

***NOTE**: Attempt <u>five</u> questions in all, including Question No. I which is compulsory, selecting two questions from each Unit.*

*x-x-x*

I. Attempt the following:-

a) Explain how a package is designed for wireless applications?

b) In digital circuit testing, compare the parallel simulation and concurrent simulation.

c) What is a D-algorithm? Compare it with PODEM algorithm.

d) What are delay faults? How can they be tested?

e) Compare the working of LP SR and MISR in BIST (5x2)

## UNIT - I

II. Explain why a die is packaged after fabrication process? What are the current trends in packaging? Explain how the packaging technology has evolved? (10)

III. What are the sources of moisture in a package? What changes are required in packaging technology to control the moisture? Explain such packages in detail. (10)

IV. Write notes on:-

a) Fault modeling

b) Fault simulation (5,5)

## UNIT - II

V. a) Why testing of VLSI chip is required? How the test patterns are generated?

b) Explain the salient features of ATPG algorithm. Discuss its types and compare it with PODEM algorithm. (3,7)

VI. Explain how boundary scan technique is used in the testing of microelectronic chips? How it is compared with BIST technique? What is BSDL? (10)

VII. Write notes on:-

a) Testable combinational logic circuit design

b) Test algorithms for RAM circuits (5,5)

*x-x-x*