Exam.Code:0935 Sub. Code: 6982

2021

B.E. (Electrical and Electronics Engineering) Fifth Semester EE-510: Microcontrollers

Time allowed: 3 Hours Max. Marks: 50

NOTE: Attempt <u>five</u> questions in all, including Question No. I which is compulsory and selecting two questions from each Unit.

X-X-X

- I. Attempt the following:
 - a) What is the function of the instruction CJNE.
 - b) Explain the difference between CISC and RISC processor.
 - c) What is the advantage of Register Indirect Addressing Mode?
 - d) How many banks are present in PIC18 & what is the size of each bank.
 - e) Distinguish between Von Neumann and Harvard Architecture.

(5x2)

UNIT - I

- II. a) WAP to exchange the lower nibble with a higher nibble for a series of 20 numbers starting at address 50H and then place the numbers at address 70 H onwards.
 - b) WAP to receive the data which has been sent in serial form at Baud rate 19200 and subsequently to send it to port2 in parallel form. (5,5)
- III. a) Twenty numbers are stored in RAM location 50H onwards. WAP to eliminate all the blanks in this set and save the rest at 70H address onwards.
 - b) Discuss the SFRs used in Interrupt process of 8051? (5,5)
- IV. a) WAP to receive the data which has been sent in serial form and send it Out to port 0 in parallel form. Also save the data at Ram location 70H. Use Timer 1 in mode 2 and 9600 baud.
 - b) Explain LCD interfacing with 8051.(only the hardware design). How is the Busy Flag checked? (5,5)

<u>UNIT – II</u>

- V. a) Discuss the addressing of Program memory and Data memory in PIC 18.
 - b) Discuss CALL instruction with reference to PIC 18.

(5,5)

- VI. a) Explain the concept and advantage of Pipelining in PIC 18.
 - b) In the instruction "GOTO target-addr" explain why the lowest bit of Program counter is 0.
 - c) Specify the expected result in W register of PIC 18 for the instructions: MOVLW 0 X 65

ANDLW 0 X 76

(4,4,2)

- VII. Write short notes on the following:
 - a) Keyboard Debouncing
 - b) Memory mapping
 - c) Interrupt service Routine
 - d) Stepper Motor
 - e) Nested Subroutines

(5x2)