Exam.Code:0929 Sub. Code: 6913

## 2021

## B.E. (Electronics and Communication Engineering) Fifth Semester

EC-505: Digital System Design

Time allowed: 3 Hours

Max. Marks: 50

**NOTE**: Attempt <u>five</u> questions in all, including Question No. I which is compulsory and selecting two questions from each Unit. Use of scientific calculator is allowed. x-x-x

- I. Attempt all questions:
  - a) What are essential prime implicants with suitable example?
  - b) What must be the minimum distance for a code to be an error detecting code?
  - c) Describe the pulse mode and explain how it is different from the fundamental mode.
  - d) Discuss critical Races in digital circuits.
  - e) What do you mean by distinguishing sequences?

(5x2)

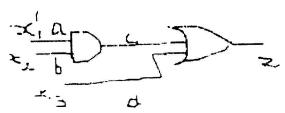
## UNIT - I

II. Minimize the following multiple output function.

$$F_{1}(X_{1}, X_{2}, X_{3}, X_{4}) = \Sigma(2,3, 4,5,6,7,11,14) + d \Sigma (9,10,13,15)$$

$$F_{2}(X_{1}, X_{2}, X_{3}, X_{4}) = \Sigma (0, 1,3,4,5,7,11,14) + d \Sigma (8,10,12,13)$$
(10)

- III. a) Find the systematic and Nonsystematic cyclic code for message 1010. Given  $g(x) = X^3 + X^2 + 1$ .
  - b) What are different properties of Boolean difference method for fault detection and location. (2x5)
- IV. a) Find the essential test vectors in the following logic diagram by using Fault table method.



b) Design full adder using two half adders and OR gate.

(2x5) P.T.O.

## <u>UNIT - II</u>

- V. Design asynchronous sequential circuit with two inputs X and Y and with one output Z. When Y=1, input X is transferred to Z. When Y is 0, the output doesn't change for any change in X. Use SR latch for implementation of the circuit, (10)
- VI. a) Explain Races and Cycles in asynchronous sequential circuit.
  - b) Determine a minimal state table equivalent to the state table given:

Next State, Output	
X=0	X=I
1,0	1,0
1,1	6,1
4,0	5,0
1,1	7,0
2,0	3,0
4,0	5.0
2,0	3,0
	X=0 1,0 1,1 4,0 1,1 2,0 4,0

(2x5)

VII. Design a sequence detector to detect sequence 100011 by using JK flip flop. (10)