Exam.Code:0929
Sub. Code: 6910

2021

B.E. (Electronics and Communication Engineering)

Fifth Semester

EC-502: Digital Signal Processing

Time allowed: 3 Hours Max. Marks: 50

***NOTE**: Attempt <u>five</u> questions in all, including Question No. I which is compulsory and selecting two questions from each Section.*

x-x-x

1. a. Define aliasing. How aliasing can be reduced?
   b. What are the effects of finite word length in digital filters?
   c. Describe the MAC operation in TMS320Cxx processor.
   d. Explain the relation between the z-transform and DFT.
   e. Determine whether given signal is periodic. If a signal is periodic, find its fundamental period and fundamental frequency. $x(n) = \cos\frac{1}{2}n$ (5×2)

Section A

2. a. Describe time frequency analysis of signals using wavelet transforms. How increasing frequency resolution does decreases time resolution.
   b. Derive the DFT of the sample data sequence
   $$x(n) = \{\tfrac{1}{5} \ for-1 \le n \le 1; \quad 0, otherwise\}$$ (5+5)

3. a. Given $x(n) = \{0,1,2,3\}$, find $X(k)$ using DIT FFT algorithm.
   b. Determine the causal signal $x(n)$ having the z-transform using partial fraction method
   $$X(z) = \frac{1}{(1+z^{-1})(1-z^{-1})^2}$$ (5+5)

4. Find the response of an FIR filter with impulse response h(n) = {1,2,4} to the input sequence x(n) = {1,2} using linear and circular convolution. Compare the results.(10)

Section B

5. a. Describe the frequency domain analysis of Decimator. What are the effects of decimation on frequency spectrum of the signal?
   b. Determine the edge frequencies, order of the filter and -3dB cut-off frequency for a Butterworth filter satisfying following constraints
   $$\sqrt{0.5} \le |H(e^{jw})| \le 1 \qquad 0 \le w \le \pi/2$$
   $$|H(e^{jw})| \le 0.2 \qquad 3\pi/4 \le w \le \pi$$
   with T = 1s. (5+5)

6. a. Name the different types of window functions. How they are defined?
   b. Obtain the cascade realization of the system characterized by the transfer function
   $$H(z) = \frac{2(z+2)}{z(z-0.1)(z+0.5)(z+0.4)}$$ (5+5)

7. a. Apply bilinear transformation to $H(s) = \frac{2}{(s+1)(s+3)}$ with T = 0.1s.
   b. Discuss the architecture of TMS320CXX series processor and also discuss the addressing modes of TMS320C5X processor. (5+5)

x-x-x