Exam.Code:0929
Sub. Code: 6909

2021

B.E. (Electronics and Communication Engineering)

Fifth Semester

EC-501: VLSI Design

Time allowed: 3 Hours | Max. Marks: 50

***NOTE**: Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Section. Use of scientific calculator is allowed.*

x-x-x

Q1. Answer the following:-

(a) What is seed crystal? (1)

(b) Why arsenic is best n-type dopant but not used? (1)

(c) Why wet oxidation process is preferred for masking oxide preparation? (1)

(d) Why high value of inductance cannot be made on IC? (1)

(e) Why anodic oxidation is not preferred over thermal oxidation process in MOS fabrication? (1)

(f) The channel region of majority carriers exists in accumulation region but MOSFET is not used for switching purpose, Why? (1)

(g) What is hot electron effect and its significance in short channel MOSFET? (1)

(h) What is the difference between dopant and carrier concentrations? (1)

(i) What is Euler's path and how it is beneficial in stick diagram design? (1)

(j) What is the body bias effect in MOSFET? (1)

SECTION A

Q2. (a) Derive the equation of maximum attainable pull rate in Czochralski process of crystal growth. (5)

(b) Discuss and compare diffusion and ion implantation process. (5)

Q3. (a) What are the disadvantages of optical lithography? Discuss the differences between positive and negative photo-resist. (5)

(b) What is positive and negative photo-resist? Which one is preferred and why? (5)

Q4. (a) Why the (111) plane is not preferred for the fabrication of the MOS transistors? (3)

(b) Why oxidation is faster for (111) plane than (100) plane? (2)

(c) What is annealing and its importance in ion implantation process? (5)

SECTION B

Q5. (a) Calculate equivalent W/L of the two nMOS with aspect ratios W_1/L and W_2/L connected in (i) Series, (ii) Parallel. Ignore body bias effects. (5)

(b) Discuss the current technological advancement as the conventional MOSFET designs are now obsolete. (5)

Q6. (a) Design a resistive-load inverter with R = 1 kΩ, such that V_{OL} = 0.6 V. The enhancement-type nMOS driver transistor has the parameters: V_{DD} = 5.0 V, V_{To} = 1.0 V, $\gamma = 0.2\ V^{1/2}$, $\lambda = 0$, $\mu_n C_{ox} = 22.0\ \mu A/V^2$ (5)

(a) Determine the required aspect ratio, W/L.

(b) Determine V_{IL} and V_{IH}.

(c) Determine noise margins NM_L and NM_H.

(b) Design a Boolean function F = ABC+AC+BC using transmission gate. (5)

Q7. Design the master slave D-flip flop circuit using transmission gate. (10)

x-x-x