Exam.Code:0977
Sub. Code: 7435

2021
M. Tech. (Micro-Electronics)
Third Semester
MIC-301: Low Power Digital CMOS Design

Time allowed: 3 Hours Max. Marks: 50

NOTE: *Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Unit.*

x-x-x

I. Attempt the following:-

a) What are material limits and device limits for low power design of digital circuits?

b) Discuss the types of power consumption in digital circuits.

c) Differentiate between 4T and 6T SRAM cell.

d) Discuss techniques to reduce power in digital circuits.

e) What is inter signal co-relations? Explain. (5x2)

UNIT – I

II. Explain the concept of low power design in VLSI CMOS circuits. What are the major challenges in the low power digital design? What are the major applications of low power circuits in microelectronic research? (10)

III. a) What are the sources of power dissipation in MOSFETs? What are the models which include the low power operation of a MOSFET?

b) Discuss how the power can be estimated in a low power designed circuit. (6,4)

IV. Write notes on:-

a) Signal statistics

b) Leakage component of power (5,5)

UNIT – II

V. a) Discuss and compare the banked organization and divided word line architecture techniques of low power design in static SRAM architectures.

b) Discuss the steps to design a sense amplifier circuit for an SRAM. (5,5)

P.T.O.

VI. a) Explain how power is distributed into various parts in a CMOS digital VLSI chip? What is the influence of technology scaling on power dissipation?

b) Explain how the low power circuits are tested? (7,3)

VII. Write notes on:-

a) Predictive shutdown approaches for low power

b) Low power write driver circuit design (5,5)

x-x-x